27.4 Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE-Mode Piezoelectric Energy Harvesting of Multi-Axial Human Motion

Miao Meng[1], Ahmed Ibrahim[1], Tiancheng Xue[2], Hong Goo Yeo[3], Dixiong Wang[1], Shad Roundy[2], Susan Trolier-McKinstry[1], Mehdi Kiani[1]

[1]Pennsylvania State University, University Park, PA
[2]University of Utah, Salt Lake City, UT
[3]Daegu- Gyeongbuk Institute of Science and Technology, Daegu, Korea

The past few years have witnessed a growing demand for self-powered wearables that can enable vigilant health monitoring, with 24/7 operation. Energy harvesting from human-body motion is attractive for wearables; however, conventional unidirectional single-cantilever-beam piezoelectric energy harvesters (PEHs) [1-4] suffer from several body-motion harvesting challenges: such as multi-axial motion, irregular frequencies, and unpredictable amplitudes with frequent low-power levels [5]. To address these challenges, an eccentric rotor-based inertial PEH has been developed, which utilizes multiple magnetically plucked flexible thin-film (60μm) PZT-nickel-PZT beams to significantly increase the harvested energy within a small volume [5]; compared to bulk-PZT beams that are more feasible in direct-force-driven PEHs. The wrist-worn multi-beam PEH, shown in Fig. 27.4.1, converts multi-axial body motion into AC voltages with different phases and decaying amplitudes (up to several volts) within the frequency range of 90-160Hz for each beam.

Current PEHs, utilizing synchronized-switch harvesting on inductor (SSHI) [1], energy investing [2], and synchronous electrical charge extraction (SECE) [3,4], suffer from multiple shortcomings: (1) they can only interface to one beam; (2) SSHI and SECE inherently suffer from harvesting shock responses and large inputs (large power loss in inductor), respectively; and (3) SECE with passive negative-voltage converters (NVCs) suffers from harvesting low PEH voltages, which often occur due to body motion. This paper presents a PEH chip (Fig. 27.4.1) with five unique capabilities: (1) simultaneous energy harvesting from up to 6 piezoelectric beams in a modular fashion using a single shared off-chip inductor; (2) seamless self-reconfiguration between operating as an efficient full-wave active rectifier (voltage mode, VM) or as an SECE to improve overall efficiency, extract the maximum energy, and to protect the chip against large inputs; thus, eliminating the need for off-chip components [3] or the use of a high-voltage process [4]; (3) extension of the input-voltage range (as low as 35mV) by utilizing active NVCs; (4) adaptive SECE operation (peak and zero-crossing time detection) to address the input frequency and beam variation; and (5) an optimal cold start (self-starting) with a tiny active-voltage doubler. Fig. 27.4.1 shows a block diagram of the proposed chip including 6 identical full-wave active rectifiers with active NVCs (VM: one per beam), a shared SECE circuit for 6 beams, a control circuit for optimal switching and reconfiguration, and a voltage doubler connected to an additional 7th beam (only for startup when active NVCs cannot operate). The chip externally requires one inductor (L_{EXT}), one storage capacitor (C_{STORE}) generating V_{STORE}, and one cold-start capacitor (C_{CHIP}), which with the beam's internal capacitance (C_P) forms a voltage doubler (eliminating one external capacitor) to supply the chip's internal circuitry via V_{CHIP}.

As shown in Fig. 27.4.1, the outputs from the beams ($V_{P,n}$) are first full-wave rectified by the active NVCs, generating $V_{REC,n} \approx |V_{P,n}|$, where n is the beam number, 1-6. As long as $V_{REC,n} < V_{STORE}$ beam-n's active rectifier is off ($P_{1,n}$:OFF), and $C_{P,n}$ is charged by the beam's internal current ($I_{P,n}$). Figure 27.4.2 shows key operational waveforms for the proposed reconfigurable VM-SECE scheme. When the peak $V_{REC,n} > V_{STORE}$, the chip seamlessly transitions between VM and SECE operation. Otherwise, the chip operates only based on SECE. For VM-SECE operation, when $V_{REC,n}$ slightly surpasses V_{STORE}, $P_{1,n}$ turns on, charging C_{STORE} with a high efficiency (95.6%), via $I_{P,n}$ (called VM), until $I_{P,n}$ reaches zero. At which time, $V_{REC,n}$ goes slightly below V_{STORE}, turning $P_{1,n}$ off and triggering SECE, which is time multiplexed for the 6 beams. Similar to a conventional SECE [4], the remaining stored energy in $C_{P,n}$ is extracted by first transferring it to L_{EXT} for a short time period by enabling $SW_{1,n}$ (transmission gate $TG_{1,n}$:ON) and SW_2 (N_1:ON) and disabling SW_3 (N_2:OFF) until $V_{REC,n}$ reduces to zero. Then L_{EXT} energy is transferred to C_{STORE} via a diode (P_2) by disabling $SW_{1,n}$, SW_2 ($TG_{1,n}$, N_1:OFF) and enabling SW_3 (N_2:ON). If the peak $V_{REC,n} < V_{STORE,}$ the chip adaptively skips VM, and only operates in SECE; by following the same protocol except that SECE is triggered by $V_{REC,n}$ peak instead of $I_{P,n}$ zero-crossing time (rising edge of $V_{VM,n}$). Employing VM not only improves overall efficiency, but it also limits the beams' voltages to $\approx V_{STORE}$, i.e., efficient over-voltage protection. Figure 27.4.2 also shows key waveforms for asynchronous and synchronous inputs. For synchronous inputs (worst case), VM operations occur simultaneously via their own paths, while the shared SECE is time multiplexed between beams with minimal loss since SECE operation requires only 50μs relative to the inputs' lower frequency (90-160Hz).

Figure 27.4.3 shows schematic diagrams for the active NVC and control block: which includes a multi-beam sweep, peak and zero-crossing time detection (PKD&ZCD), and switching control. In the NVC a comparator switches pass transistors to full-wave rectify the input actively with a minimal voltage drop. Within a multi-beam sweep, the beams' voltages ($V_{P,n}$) are checked one-by-one every 60μs in a loop by 6 cascaded beam-control blocks. There are 4 possible conditions: (1) $C_{P,n}$ is charging, $V_{REC,n} < V_{STORE}$, (2) C_{STORE} is charging via VM, $V_{REC,n} > V_{STORE}$, (3) VM operation has ended ($V_{VM,n}$ is high) with some charge left on $C_{P,n}$, and (4) $V_{REC,n}$ reaches its peak, $V_{REC,n} < V_{STORE}$. Under conditions 1 and 2 (PKD_n=0), beam-n is skipped through flip-flop $FF_{2,n}$ followed by a 60μs delay to check the next beam. Under conditions 3 and 4 (PKD_n=1), SECE immediately starts and beam control waits until SECE operation ends, i.e., $SW_{1,n}$ goes low to clock $FF_{1,n}$, triggering the next beam after 60μs. In PKD&ZCD, a positive edge is generated at $V_{REC,n}$ peak and combined with $V_{VM,n}$ to clock a flip-flop for generating high PKD_n (indicating the start of SECE), which is reset to low at $V_{REC,n}$ zero-crossing time (ZCD_n=1). Finally, switching control generates required $SW_{1,1\text{-}6}$, SW_2 and SW_3 signals.

The proposed chip was fabricated in a 0.35μm 4M-2P standard-CMOS process, occupying 1.9mm^2 of active area. The chip was integrated with the inertial harvester (6 beams for charging C_{STORE}, and 1 beam for cold start), as shown in Fig. 27.4.1. In all measurements, L_{EXT} = 2.2mH, C_{STORE} = 47μF, C_{CHIP} = 10μF. Figure 27.4.4 shows the chip's measured transient waveforms, when the inertial harvester is gently shaken. During a cold start, C_{CHIP} was first charged via P_{C2} in Fig. 27.4.1 in a passive manner to ≈1.5V. At which point, the active voltage doubler starts to operate, charging C_{CHIP} efficiently to V_{CHIP} = 3.2V, with a $V_{P,7}$ peak-to-peak voltage as large as 4V. Similarly for $V_{CHIP} < 1.5$V, C_{STORE} is charged via the 6 $P_{1,n}$ transistors in a passive manner to ≈1.5V. At which point, the active rectifiers in VM start to operate, further charging C_{STORE} to ≈1.9V via VM, for $V_{CHIP} < 3$V (chip not fully functional yet). When $V_{CHIP} > 3$V, then the chip operates in the reconfigurable VM-SECE mode (fully-functional) to charge C_{STORE} more efficiently (at a faster rate in Fig. 27.4.4) to $V_{STORE} > 1.9$V in the presence of different voltage/frequency variations on each beam.

Figure 27.4.5 shows how the chip improves stored power (P_{STORE}) vs. V_{STORE} for weak periodic and shock vibrations to a single beam (open-circuit voltage, $V_{P,OC}$ = 1.6V). The chip (reconfigurable VM-SECE) harvested 2.43× and 3.65× more power than the maximum energy harvested using the 95.6%-efficient full-wave active rectifier (on-chip VM) for periodic and shock vibrations, respectively. Note, that due to the low-frequency operation, offset compensation is not required. This leads to a high shock figure-of-merit (FoM): 365% for a single beam. Utilizing all 6 beams, the FoM further increases to 511% because VM-SECE scheme can extract almost all of the energy from the individual beams, regardless of their voltage levels. Whereas, 6-parallel active rectifiers cannot. The table in Fig. 27.4.6 benchmarks our chip against the prior-art. This chip provides an adaptive reconfigurable VM-SECE scheme that maximizes efficiency and the extracted power for a wide range of inputs. It can interface 6 beams in a modular fashion, with inputs as low as 35mV. Allowing it to harvest energy from multi-axial body motion, which is often weak, using multiple flexible thin-film beams.

References:

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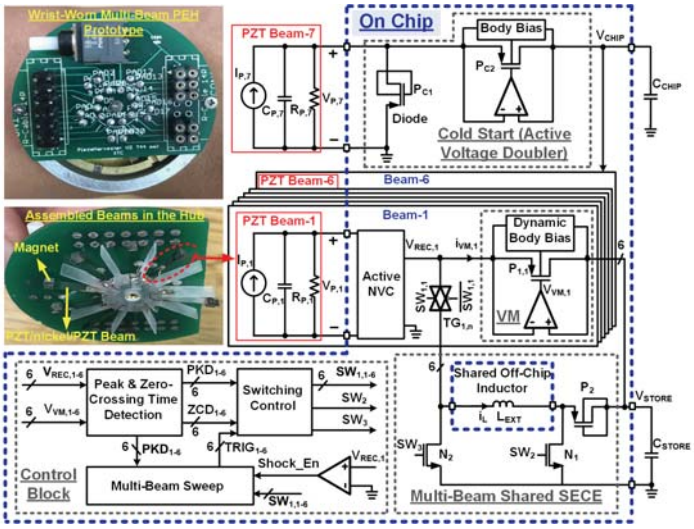

Figure 27.4.1: Wrist-worn multi-beam PEH prototype and block diagram of the proposed chip.

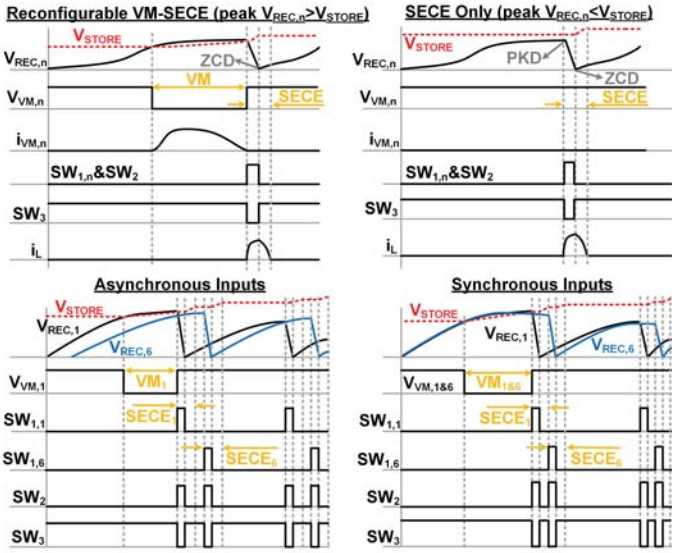

Figure 27.4.2: Key operational waveforms of the proposed chip.

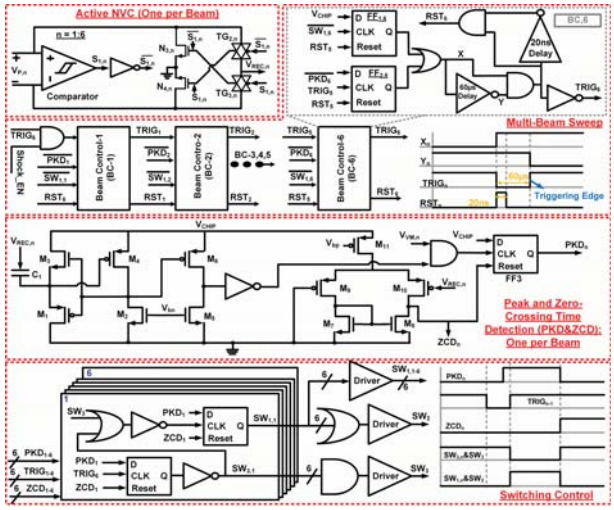

Figure 27.4.3: Schematic diagrams of the active NVC and control block: including a multi-beam sweep, peak and zero-crossing time detection, and switching control.

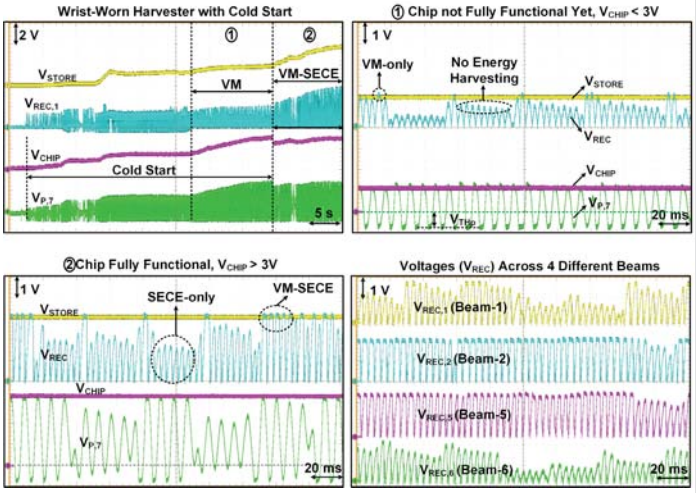

Figure 27.4.4: Measured transient waveforms of the proposed chip interfacing with a wrist-worn multi-beam PEH.

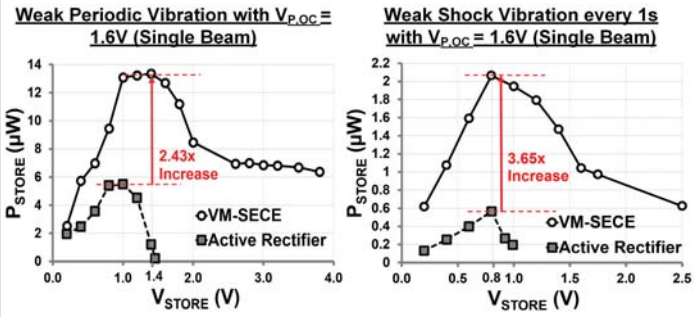

Figure 27.4.5: Comparison of measured harvested power (P_{STORE}) vs. V_{STORE} for a single beam between our VM-SECE chip and a full-wave active rectifier (on-chip VM-only) for weak periodic and shock excitations ($V_{P,OC}$ = 1.6V). For stronger vibrations with $V_{P,OC}$ = 2V, the harvested power increased by 1.6× on average.

Publication	[1]	[2]	[3]	[4]	This work
CMOS Tech (nm)	350	350	350	40 (10V)	350 (5V)
Chip Size (mm²)	0.72	2.34	3.6	0.55	1.9
Scheme Type	SSHI	Energy Investing	Multi-Shot SECE	SECE	Reconfigurable VM-SECE
# of Beams (Inputs)	1	1	1	1	6 (Modular)
Piezoelectric Energy Harvester	MIDE V21B & V22B	MIDE V22B	Murata	MIDE PPA1011	Custom PZT/nickel/ PZT (Wrist-Worn)
C_P (nF)	26	15	23	43	17-49
Beam Dimension, l×w×t (mm)	6.25 × 1.5 × 0.7	6.25 × 1.5 × 0.7	-	71 × 25.4 × 0.7	12 × 3 × 0.06 (each beam, flexible)
Excitation Type	Periodic & Shock	Periodic	Periodic	Periodic & Shock	Multi-Axial Body Motion
Operation Freq. (Hz)	225	143	100	75.4	90-160
FoM* (%) @ $V_{P,OC}$ (V)	269 @ 2.5	-	-	330 @ 3.4	1-Beam: 365 @ 1.6 6-Beam: 511 @ 1.6
Cold Startup	Yes	No	Yes	Yes	Yes
Maximum End-to-end Efficiency (%)	≈88**	69.2	61	94	VM: 95.6 VM-SECE: 84.6
Minimum Input Voltage (mV)	670	570	-	-	35
Quiescent Current (μA)	1	0.1	0.3	0.03	0.5 (6 beams)

*FoM = max(P_{out})/max($P_{out,FAR}$) for shock input (FAR: Full-wave active rectifier). **Calculated.

Figure 27.4.6: Comparison table of this work to prior-art.

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1	Cold Start
2	Beta Multiplier (Current Reference)
3	Active Negative Voltage Converter (NVC)
4	Power-Path Switches
5	Voltage Mode (VM)
6	Peak and Zero-Crossing Time Detection (PKD&ZCD)
7	Switching Control
8	Multi-Beam Sweep
9	Shock Detection

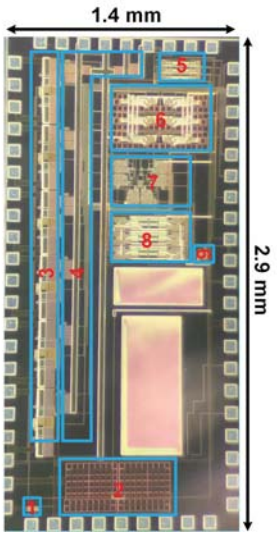

Figure 27.4.7: Proposed chip micrograph, occupying 1.9mm² of active area, and its key building blocks.

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