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ABSTRACT

Ferroelectric semiconductor field effect transistors (FeSmFETs), which employ ferroelectric semiconducting thin crystals of α-In_2Se_3 as the channel material as opposed to the gate dielectric in conventional ferroelectric FETs (FeFETs), were prepared and measured from room to liquid-helium temperatures. These FeSmFETs were found to yield evidence for the reorientation of electrical polarization and an electric field-induced metallic state in α-In_2Se_3. Our findings suggest that FeSmFETs can serve as a platform for the fundamental study of ferroelectric metals as well as the exploration of potential applications of semiconducting ferroelectrics.

Ferroelectricity is defined by the formation of spontaneous electrical polarization in a non-centrosymmetric crystal and the reorientation of the polarization between crystallographically defined directions by the application of an external electric field.[1] Ferroelectrics have been used to store data in either a capacitor or a ferroelectric field-effect transistor (FeFET)[2,3] configuration, the latter of which features a ferroelectric gate dielectric and a non-ferroelectric semiconducting channel. FeFETs provide not only fast and non-volatile data storage but also a pathway toward "logic in memory" functions. However, the commercialization of FeFETs has encountered multiple obstacles ranging from the retention time originating from the depolarization field and the gate leakage current[4] to endurance limited mainly by interface charge traps.[5] A FeFET variation, which replaces the semiconducting channel in the conventional FET with a *ferroelectric* semiconducting channel but retains the non-ferroelectric gate dielectric, was demonstrated recently.[6] This produces an "on" (or "off") state without an applied gate voltage, similar to a traditional FeFET. Such a device is referred to as a ferroelectric semiconductor field effect transistor (FeSmFET).

It is interesting to ask whether the "on" state in the FeSmFET can be a metallic state, which will make the transition from the "on" to the "off" state a ferroelectric metal-insulator transition. Anderson and Blount[7] examined the structural transition found in metallic V_3Si and suggested that the formation of ionic displacements along a polar axis, which led to the loss of inversion symmetry, would be required for the occurrence of the apparent continuous phase transition seen in V_3Si. Furthermore, they suggested that such a state should be called a "ferroelectric metal." Being a metal appears to be inconsistent with the accepted definition of ferroelectricity as mobile charge carriers in a bulk metal will effectively screen any electric field, making the reorientation of the polarization unlikely. Nevertheless, metals showing the presence of electrical dipoles from ionic displacements along with a well-defined polar axis, such as $LiOsO_3$,[8,9] $Ca_3Ru_2O_7$,[10] and other materials,[11] have attracted much attention in recent years even though the issue of whether the dipoles found in these materials are spontaneously ordered and reversible has not been resolved. Interestingly, the difficulty in reversing the polarization in a metal can be circumvented for a ferroelectric 2D crystal. A vertical electrical field, applied to a 2D crystal of 1T′-WTe_2 by a top and a bottom gate, was shown to lead to sharp jumps in sample conductance, which was attributed to polarization reversal.[12] However, direct evidence for ferroelectricity in 2D 1T′-WTe_2 is still lacking.

In_2Se_3, a layered transition metal chalcogenide (TMC) featuring a van der Waals interlayer coupling and an energy gap of 1.4 eV, was

predicted[13] to be ferroelectric down to a 1-unit-cell thickness in both α- and β-phases. Supporting evidence for ferroelectricity in In_2Se_3 was found via piezoelectric force microscopy (PFM)[14–18] and second harmonic generation (SHG),[18–20] with a transition temperature up to 700 K.[19] Extensive device work carried out in the last few years also supports ferroelectricity in this layered TMC. An on/off state was found in rectifying devices by sweeping the source-drain voltage,[14–17,21] revealing distinct hysteresis loops suggesting complex orientations of the polarization.[14,16,19] In the pioneering work of the FeSmFET featuring thin crystals of α-In_2Se_3 and a gate dielectric of 90-nm-thick SiO_2 or 15-nm-thick HfO_2, respectively, large clockwise and counterclockwise hysteresis loops were found in gate voltage sweeps.[6] The hysteresis was shown to persist down to 80 mK, making it unlikely that the observed hysteresis at such a low temperature is due to charge traps. These observations strongly support the existence of ferroelectricity in α-In_2Se_3. However, the most explicit demonstration of ferroelectricity in α-In_2Se_3 was obtained in a stacked capacitor/FET device.[22] This device consists of monolayer graphene on a SiO_2/Si substrate that functions as a bottom gate. Graphene is also the bottom electrode for a capacitor featuring a two-layer dielectric combining an insulating monolayer or bilayer of hexagonal boron nitride (hBN) and an atomically thin, semiconducting crystal of α-In_2Se_3, which was covered by a top metal electrode/gate. The electric field applied between graphene and the top electrode was used to reorient the polarization in α-In_2Se_3. Graphene sandwiched between SiO_2 and hBN functioned as a charge detector through the position of the charge neutral point (CNP) in sample resistance vs the gate voltage curves. From the clear and systematic shift in the CNP as the polarization was flipped, a polarization value of 0.92 $\mu C/cm^2$ was estimated under an external field of 5×10^5 V/cm, which is reasonably close to the theoretically predicted[13] value of 0.6 $\mu C/cm^2$.

The in- and out-of-plane resistivities of α-In_2Se_3 crystals grown by a modified Bridgman method used in this work, obtained from a four-point probe on bulk crystals using electrical contacts made by Ag paint, showed a variable-range hopping (VRH) conduction at low temperatures [below ~40 K, see Fig. 1(a)] after the unintentionally doped charge carriers are frozen out. Thin crystals of α-In_2Se_3 were obtained by mechanical exfoliation from a bulk crystal and deposited onto a heavily doped silicon chip with a 300-nm thick thermally grown surface of SiO_2. The thickness of a thin crystal of α-In_2Se_3 was determined by atomic force microscopy (AFM) after the transport measurements were carried out. Two types of FeSmFETs featuring a Hall bar [Fig. 1(e)] and traditional FET [Fig. S1(a) in the supplementary material] pattern, respectively, were prepared by photolithography with electrodes of 5 nm of Ti and 45 nm of Au. The parameters for the four devices used in the present study are shown in Table S1 in the supplementary material. DC electrical transport measurements were carried out using a Quantum Design Physical Property Measurement System (PPMS) equipped with a 9 T superconducting magnet that features a base temperature of 1.8 K. For temperature varying measurements, the device was cooled/warmed at zero gate voltage unless otherwise specified.

To characterize the thin crystals of α-In_2Se_3, Raman spectroscopy, photoluminescence (PL) and second harmonic generation (SHG) measurements were used. The Raman spectra [Fig. 1(b)] confirmed that the crystals used were α-In_2Se_3.[23] An energy gap value of 1.4 eV was revealed in the PL measurements [Fig. 1(c)], consistent

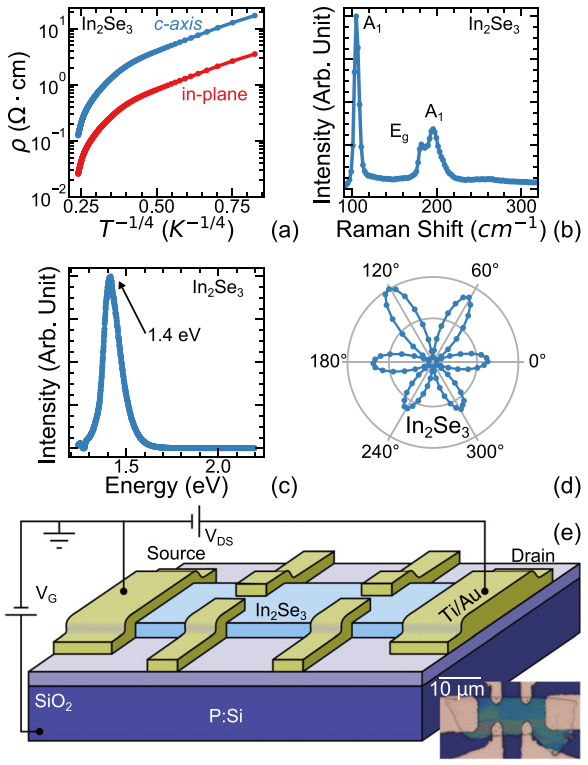

FIG. 1. (a) In- and out-of-plane resistivities of bulk single-crystals α-In_2Se_3 showing Mott variable-range hopping conduction behavior, $\rho_{\text{in-plane, c-axis}}(T) \sim \exp[(T_0/T)^{1/4}]$, where T_0 is a constant, below around $T = 160$ K. Also shown are results of Raman spectroscopy (b), photoluminescence (c), and second harmonic generation (d) measurements. A schematic of an FeSmFET in the Hall bar pattern is shown in (e). Inset: optical image of a FeSmFET device following this design with the 10-μm scale bar also shown.

with that found in the literature.[23] Strong SHG signals with the expected sixfold symmetry were also found [Fig. 1(d)], demonstrating that our α-In_2Se_3 crystal indeed belongs to the *R3m* space group.[17–19]

Source-drain current vs voltage (I_D vs V_{DS}) characteristics were measured on the FeSmFETs at fixed gate voltages (V_G). The results for sample A [Fig. 1(e)] with a channel length of 12 μm and a thickness of 110 nm are shown in Fig. 2 for V_G increasing from −75 to 75 V and back to −75 V. No saturation in I_D was observed in this range of gate voltages up to 10 V for all V_G values. Given that I_D for negative V_G is lower than I_D for the positive, α-In_2Se_3 must be *n*-type, consistent with previous observations.[24,25] Similar features in I_D vs V_{DS} characteristics were seen in other samples (Fig. S2). Interestingly, a marked change in the slope was found in most I_D vs V_{DS} curves, showing that I_D increases much faster at low V_{DS} than that at high V_{DS} values. The sharp rise in I_D at low V_{DS} values (below a few tenth of volts) may be related to the presence of two back-to-back Schottky diodes studied previously in other materials.[26,27] Behavior seen at high V_{DS} values, in particular, in the linear plots (Figs. S2 and S3), is similar to that reported previously.[6]

Clockwise transfer curves of I_D vs V_G, starting at $V_G = -75$ V, were measured on our FeSmFET devices at fixed temperatures, *T*, from 300 to 2 K (Figs. 3 and S5). These results are consistent with

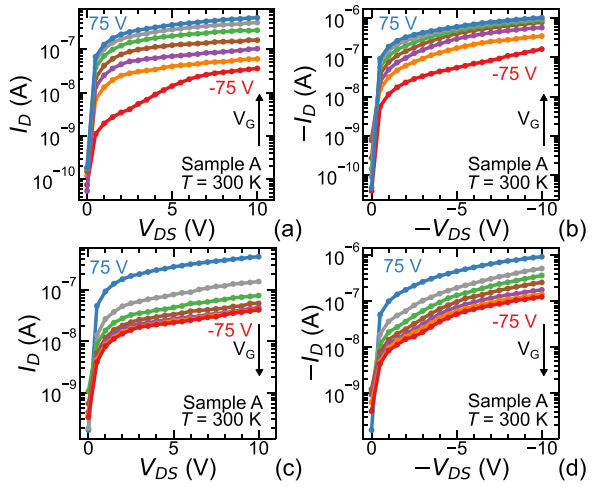

FIG. 2. Curves of I_D-V_{DS} for sample A obtained at room temperature for fixed gate voltages in an increasing order, $V_G = -75, -50, -25, 0, 25, 50, 75$ V at positive (a) and negative (b) values of V_{DS}. Corresponding I_D-V_{DS} curves for decreasing V_G at the same gate voltages are shown in (c) and (d).

those seen in the previous work.[6] The clockwise hysteresis loop points to the presence of a polarization in the *n*-type α-In_2Se_3 semiconductor. Basically, at a sufficiently large negative V_G, say, −75 V, the downward pointing electric field will force the polarization inside the α-In_2Se_3 crystal downward (Fig. S1), resulting in *positive* bound surface charge on the *bottom* surface of the crystal due to the presence of the polarization. Consequently, the energy bands will band upward (Fig. S1). The gate voltage-induced *positive* charge carriers will deplete the conduction band (the existing negative charge carriers will be "drained" from the channel), which will shut down conduction channels between the source and the drain. On the *top* of the α-In_2Se_3 crystal, however, the *negative* bound charge from the downward pointing polarization will push down the conduction band, placing the Fermi energy within the conduction band (Fig. S1). However, even though the low density of the gate voltage-induced *positive* charge carriers cannot deplete the conduction band fully because the gate electric field is weak on the top surface of the crystal, no conduction channel between the source and the drain is expected there either because of the low carrier density. An "off" state of the FeSmFET is, thus, expected, which was indeed observed.

As V_G increased from −75 V–0 and then 75 V, the polarization will start to reverse locally. The depletion layer on the bottom surface of the α-In_2Se_3 crystal will be reduced, helping push down the conduction band. A conduction channel between the source and the drain will eventually be established, leading to the "on" state of the FeSmFET. The device will continue to be in the "on" state as V_G is increased further to 75 V. Now, the polarization will switch to point upward so that the bound charge from the polarization will be negative on the bottom surface of the crystal, featuring negative mobile charge carriers induced by the positive gate voltage. Ramping V_G from 75 V to 0, the polarization will turn downward locally, leading to *positive* bound charge from the polarization on the *bottom* surface of the crystal. The existing and gate induced *negative* charge carriers could be bound to the *positive* surface charge from the polarization, creating

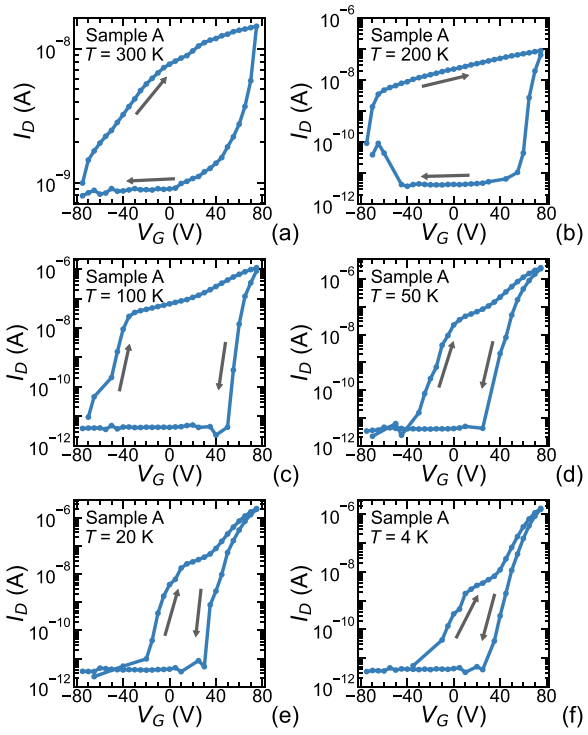

FIG. 3. (a)–(f) Transfer curves of source-drain current vs gate voltage, I_D vs V_G, obtained at fixed temperatures (T) as indicated. V_G was initially decreased from 0 to −75 V, after which V_G was ramped from –75 to 75 V and then back to –75 V, while the I_D vs V_G curve was measured. A clockwise hysteresis loop was obtained at each temperature.

local areas that are non-conducting. As the gate voltage decreases further, the polarization will continue to flip, leading to continuous growth of non-conducting areas and a decreasing I_D. Eventually, all conduction channels disappear, leading to vanishingly small I_D. A clockwise hysteresis loop as shown in Fig. 3 will be obtained. Our observation is, therefore, fully consistent with the existence of polarization in α-In_2Se_3, as argued previously.[6]

The overall hysteresis decreased as the temperature T was lowered (Fig. 3). Thus, it is natural to ask whether the reduction in hysteresis was a result of a change in the coercive field as the temperature was lowered. This seems to be unlikely given that the ferroelectric transition temperature, T_c, of α-In_2Se_3 was reported to be 700 K[19] as the coercive field of a ferroelectric material would increase as T is lowered below T_c[28,29] or remain constant far below it. The more likely scenario is the decrease in hysteresis as T was lowered was due to the presence of charge traps in our sample. Charge traps in FETs are known to lead to a hysteresis loop. At higher temperatures, the hysteresis originating from charge traps and that from polarization appear to coexist in our samples. However, at a liquid-helium temperature, at which the binding and unbinding of mobile charge carriers from their traps are expected to be suppressed, the observed hysteresis should be only due to the reversal of the polarization, as argued previously.[6]

Values of two-point resistance R_{DS} (= I_D/V_{DS}, taken from the top of the hysteresis loop) are plotted against T in Fig. 4(a), showing decreasing R_{DS} with the lowering T and the emergence of a metallic

state. The four-point sample resistance, $R(T)$, of the same crystal was also measured as a function of T [inset of Fig. 4(a)], showing that $R_{DS}(T)$ and $R(T)$ have similar behavior. This suggests that the contact resistance between Ti/Au and α-In_2Se_3, which was measured at room temperature (Fig. S7), did not make a big difference in the behavior of I_D. Data obtained for $V_G = 75$ V in samples B and C showed a positive dR/dT at higher temperatures and a complete flattening-off in $R_{DS}(T)$ down to 4 K [Figs. 4(b) and S6]. A small negative dR/dT was seen at the lowest temperatures in sample A; even at $V_G = 75$ V, the density of gate voltage-induced mobile charge carriers is the largest, which appears to be due to sample specific disorder. Weak localization in a weakly disordered metallic sample can lead to a negative dR/dT when T is sufficiently low.[30] The maximum 2D electric conductivity obtained from the four-point measurements was found to be around 80 σ_0, where $\sigma_0 = e^2/h$ ($= 4.08 \times 10^{-5}\ \Omega^{-1}$) is the quantum conductance, e is the electron charge, and h is Planck's constant. Above σ_0, a negative dR/dT is expected due to weak localization, along with positive or negative magnetoconductance (MC) depending on the strength of the spin–orbital coupling.[30] Our measurements showed positive MC at 1.8 K [Fig. 4(c)], as well as 10 K and 50 K (data not shown), consistent with the weak spin–orbital coupling expected for α-In_2Se_3. The MC data are shown in Fig. 4(c) to fit Maekawa–Fukuyama theory of 2D weak localization[31] quantitatively.

In the metallic state, the negative mobile charge carriers should be accumulated near the bottom of the α-In_2Se_3 crystal, while the rest of the crystal remains semiconducting. This layer of mobile charge will tend to screen the gate electric field, making the polarization in the semiconducting region of the crystal less affected by the gate electric field. However, as shown in the data, some polarization can still be reoriented by the field even in the metallic state. As a result, the 2D metallic sheet of electrons and the polarization must coexist in α-In_2Se_3.

The interesting question is how the bound charge of polarization on the crystal bottom will affect the accumulation of the mobile electrons. At $V_G = 75$ V, the electric field is expected to induce an electron density of $5 \times 10^{12}/cm^2$. Hall measurements showed that the Hall voltage is a linear function of the magnetic field, suggesting that only electrons are present in the sample. The density of electrons at 4 K is roughly what would be expected solely from that induced by the gate electric field, unaffected by the polarization [Fig. 4(d)]. At higher temperatures, however, the electron density obtained by the Hall measurements is larger than that induced by the gate voltage. This is reasonable, as the existing unintentionally doped electrons that are bound to the positive charge traps at low temperatures would start to be released as the temperature was raised, consistent with the observation of the broadening hysteresis noted above.

The observations presented above demonstrate a well-functioning FET with a large I_D even when gate voltage is at zero. Such a FeSmFET can be used for logic operations as well as a memory device in the microelectronic circuitry with the "logic in memory" functionalities. In addition, ultrathin α-In_2Se_3 was shown to provide a test bed for fundamental research on ferroelectric metals as well as ferroelectric metal-insulator transitions tuned by a gate voltage.

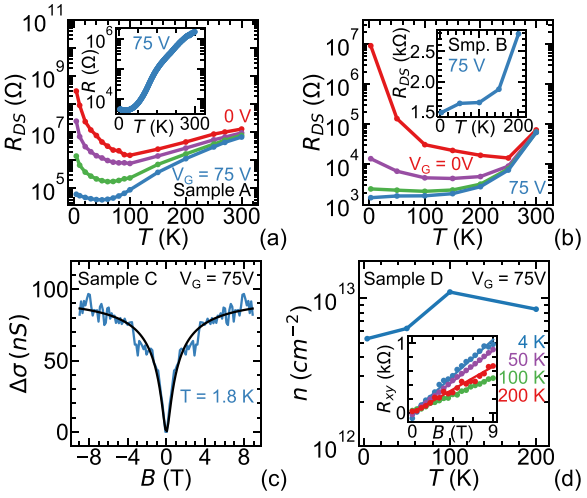

FIG. 4. (a) Two-point sample resistance, $R_{SD}(T)$ ($R_{DS} = I_D/V_{DS}$) obtained at $V_G = 0$, 25, 50, and 75 V, in the top portion of the clockwise hysteresis loops taken at fixed temperatures for sample A. Inset: four-point resistance vs temperature, $R(T)$, measured, while the device was warming up after it was cooled to 4 K at $V_G = -75$ V followed by ramping V_G from −75 to 75 V at 4 K. (b) $R_{DS}(T)$ for sample B in the semi-log plot obtained from the top portion of clockwise hysteresis loops. Inset: $R_{DS}(T)$ for $V_G = 75$ V in the linear plot. (c) Magnetoconductance at $T = 1.8$ K and $V_G = 75$ V for sample C. The Maekawa–Fukuyama theory was shown to fit the data (see the main text). (d) Charge carrier density, n, as a function of T for sample D. The device design for samples A and D is shown in Fig. 1(e), and that for samples B and C is shown in Fig. S1(a).

See the supplementary material for additional device schematics, band diagram representation, additional sample data, and device parameters.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]G. A. Smolenskiĭ, V. A. Bokov, V. A. Isupov, N. N. Krainik, R. E. Pasinkov, and I. A. Sokolov, *Ferroelectrics and Related Materials* (Gordon and Breach Science Publishers, 1984).
[2]S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Löhr, P. Polakowski, J. Müller, T. Mikolajick, J. Höntschel, B. Rice, J. Pellerin, and S. Beyer, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond," in IEEE International Electron Devices Meeting (IEDM), pp. 19.7.1–19.7.4.
[3]M. Si, P.-Y. Liao, G. Qiu, Y. Duan, and P. D. Ye, "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure," ACS Nano **12**(7), 6700–6705 (2018).
[4]T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?," IEEE Electron Device Lett. **23**(7), 386–388 (2002).
[5]W. Xiao, C. Liu, Y. Peng, S. Zheng, Q. Feng, C. Zhang, J. Zhang, Y. Hao, M. Liao, and Y. Zhou, "Memory window and endurance improvement of $Hf_{0.5}Zr_{0.5}O_2$-based FeFETs with ZrO_2 seed layers characterized by fast voltage pulse measurements," Nanoscale Res. Lett. **14**, 254 (2019).

[6]M. Si, A. K. Saha, S. Gao, G. Qiu, J. Qin, Y. Duan, J. Jian, C. Niu, H. Wang, W. Wu, S. K. Gupta, and P. D. Ye, "A ferroelectric semiconductor field-effect transistor," Nat. Electron. **2**, 580–587 (2019).
[7]P. W. Anderson and E. I. Blount, "Symmetry considerations on martensitic transformations: 'Ferroelectric' metals?," Phys. Rev. Lett. **14**(7), 217–219 (1965).
[8]Y. Shi, Y. Guo, X. Wang, A. J. Princep, D. Khalyavin, P. Manuel, Y. Michiue, A. Sato, K. Tsuda, S. Yu, M. Arai, Y. Shirako, M. Akaogi, N. Wang, K. Yamaura, and A. T. Boothroyd, "A ferroelectric-like structural transition in a metal," Nat. Mater. **12**(11), 1024–1027 (2013).
[9]N. A. Benedek and T. Birol, "'Ferroelectric' metals reexamined: Fundamental mechanisms and design considerations for new materials," J. Mater. Chem. C **4**(18), 4000–4015 (2016).
[10]S. Lei, M. Gu, D. Puggioni, G. Stone, J. Peng, J. Ge, Y. Wang, B. Wang, Y. Yuan, K. Wang, Z. Mao, J. M. Rondinelli, and V. Gopalan, "Observation of quasi-two-dimensional polar domains and ferroelastic switching in a metal, $Ca_3Ru_2O_7$," Nano Lett. **18**(5), 3088–3095 (2018).
[11]T. H. Kim, D. Puggioni, Y. Yuan, L. Xie, H. Zhou, N. Campbell, P. J. Ryan, Y. Choi, J.-W. Kim, J. R. Patzner, S. Ryu, J. P. Podkaminer, J. Irwin, Y. Ma, C. J. Fennie, M. S. Rzchowski, X. Q. Pan, V. Gopalan, J. M. Rondinelli, and C. B. Eom, "Polar metals by geometric design," Nature **533**(7601), 68–72 (2016).
[12]Z. Fei, W. Zhao, T. A. Palomaki, B. Sun, M. K. Miller, Z. Zhao, J. Yan, X. Xu, and D. H. Cobden, "Ferroelectric switching of a two-dimensional metal," Nature **560**(7718), 336–339 (2018).
[13]W. Ding, J. Zhu, Z. Wang, Y. Gao, D. Xiao, Y. Gu, Z. Zhang, and W. Zhu, "Prediction of intrinsic two-dimensional ferroelectrics in In_2Se_3 and other III_2-VI_3 van der Waals materials," Nat. Commun. **8**(1), 14956 (2017).
[14]C. Cui, W.-J. Hu, X. Yan, C. Addiego, W. Gao, Y. Wang, Z. Wang, L. Li, Y. Cheng, P. Li, X. Zhang, H. N. Alshareef, T. Wu, W. Zhu, X. Pan, and L.-J. Li, "Intercorrelated in-plane and out-of-plane ferroelectricity in ultrathin two-dimensional layered semiconductor In_2Se_3," Nano Lett. **18**(2), 1253–1258 (2018).
[15]S. Wan, Y. Li, W. Li, X. Mao, W. Zhu, and H. Zeng, "Room-temperature ferroelectricity and a switchable diode effect in two-dimensional α-In_2Se_3 thin layers," Nanoscale **10**(31), 14885–14892 (2018).
[16]P. Hou, Y. Lv, X. Zhong, and J. Wang, "α-In_2Se_3 nanoflakes modulated by ferroelectric polarization and Pt nanodots for photodetection," ACS Appl. Nano Mater. **2**(7), 4443–4450 (2019).
[17]P. Hou, S. Xing, X. Liu, C. Chen, X. Zhong, J. Wang, and X. Ouyang, "Resistive switching behavior in α-In_2Se_3 nanoflakes modulated by ferroelectric polarization and interface defects," RSC Adv. **9**(52), 30565–30569 (2019).
[18]M. Dai, K. Li, F. Wang, Y. Hu, J. Zhang, T. Zhai, B. Yang, Y. Fu, W. Cao, D. Jia, Y. Zhou, and P. Hu, "Intrinsic dipole coupling in 2D van der Waals ferroelectrics for gate-controlled switchable rectifier," Adv. Electron. Mater. **6**(2), 1900975 (2020).
[19]J. Xiao, H. Zhu, Y. Wang, W. Feng, Y. Hu, A. Dasgupta, Y. Han, Y. Wang, D. A. Muller, L. W. Martin, and P. Hu, "Intrinsic two-dimensional ferroelectricity with dipole locking," Phys. Rev. Lett. **120**(22), 227601 (2018).
[20]Y. Zhou, D. Wu, Y. Zhu, Y. Cho, Q. He, X. Yang, K. Herrera, Z. Chu, Y. Han, M. C. Downer, H. Peng, and K. Lai, "Out-of-plane piezoelectricity and ferroelectricity in layered α-In_2Se_3 nanoflakes," Nano Lett. **17**(9), 5508–5513 (2017).
[21]H. Yang, M. Xiao, Y. Cui, L. Pan, K. Zhao, and Z. Wei, "Nonvolatile memristor based on heterostructure of 2D room-temperature ferroelectric α-In_2Se_3 and WSe_2," Sci. China Inf. Sci. **62**(12), 220404 (2019).
[22]S. Wan, Y. Li, W. Li, X. Mao, C. Wang, C. Chen, J. Dong, A. Nie, J. Xiang, Z. Liu, W. Zhu, and H. Zeng, "Nonvolatile ferroelectric memory effect in ultrathin α-In_2Se_3," Adv. Funct. Mater. **29**(20), 1808606 (2019).
[23]N. Balakrishnan, E. D. Steer, E. F. Smith, Z. R. Kudrynskyi, Z. D. Kovalyuk, L. Eaves, A. Patanè, and P. H. Beton, "Epitaxial growth of γ-InSe and α, β, and γ-In_2Se_3 on ε-GaSe," 2D Mater. **5**(3), 035026 (2018).
[24]C. Julien, M. Eddrief, K. Kambas, and M. Balkanski, "Electrical and optical properties of In_2Se_3 thin films," Thin Solid Films **137**(1), 27–37 (1986).
[25]J. O. Island, S. I. Blanter, M. Buscema, H. S. J. van der Zant, and A. Castellanos-Gomez, "Gate controlled photocurrent generation mechanisms in high-gain In_2Se_3 phototransistors," Nano Lett. **15**(12), 7853–7858 (2015).
[26]R. T. Tung, "The physics and chemistry of the Schottky barrier height," Appl. Phys. Rev. **1**(1), 011304 (2014).
[27]J. Osvald, "Back-to-back connected asymmetric Schottky diodes with series resistance as a single diode," Phys. Status Solidi A **212**, 2754–2758 (2015).
[28]Z. Wang, H. Ying, W. Chern, S. Yu, M. Mourigal, J. D. Cressler, and A. I. Khan, "Cryogenic characterization of a ferroelectric field-effect-transistor," Appl. Phys. Lett. **116**(4), 042902 (2020).
[29]Y. Zhang, Z. Chen, W. Cao, and Z. Zhang, "Temperature and frequency dependence of the coercive field of $0.71PbMb_{1/3}Nb_{2/3}O_3$–$0.29PbTiO_3$ relaxor-based ferroelectric single crystal," Appl. Phys. Lett. **111**(17), 172902 (2017).
[30]P. A. Lee and T. V. Ramakrishnan, "Disordered electronic systems," Rev. Mod. Phys. **57**, 287 (1985).
[31]S. Maekawa and H. Fukuyama, "Magnetoresistance in two-dimensional disordered systems: Effects of Zeeman splitting and spin–orbit scattering," J. Phys. Soc. Jpn. **50**(8), 2516–2524 (1981).