

# A Multi-Beam Shared-Inductor Reconfigurable Voltage/SECE Mode Piezoelectric Energy Harvesting Interface Circuit

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**Abstract**—This paper presents an autonomous multi-input (multi-beam) reconfigurable power-management chip for optimal energy harvesting from weak multi-axial human motion using a multi-beam piezoelectric energy harvester (PEH). The proposed chip adaptively operates in either voltage-mode or synchronous-electrical-charge-extraction-mode (VM-SECE) to improve overall efficiency, extract maximum energy regardless of the PEH beams' impedance/voltage/frequency variations, and protect the chip against large inputs, eliminating the need for high-voltage processes. It can simultaneously harvest energy from up to 6 beams using only one shared off-chip inductor. It uses an active negative voltage converter to extend the input-voltage range to as low as 35 mV. In addition, an active voltage doubler with a small footprint is implemented for faster cold start. A prototype VM-SECE chip was fabricated in a 0.35- $\mu\text{m}$  2P4M standard CMOS process occupying 1.9 mm<sup>2</sup> active area. To fully characterize the chip performance, it was tested with both a commercial single-beam PEH and a custom-made PEH with five mechanically plucked thin-film beams. With the commercial PEH, compared to an on-chip full-wave active rectifier (FAR) with 95.6% efficiency, the VM-SECE chip harvested 3.28x more power for shock inputs at 1 Hz frequency and 4.39 g acceleration. With the custom 5-beam PEH for a pseudo-walking condition, compared to the on-chip FAR, the VM-SECE chip harvested 1.59x and 2.38x more power for 1-and 5-beam operations, respectively.

**Index Terms**—Body motion, integrated circuit, piezoelectric energy harvesting, power management, reconfigurable, synchronous electrical charge extraction (SECE), voltage mode, wearable.

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## I. INTRODUCTION

ENERGY harvesting has become more attractive over the past few years, because it promises the replacement of or complement to available batteries in wireless sensor networks (WSNs) [1]. A typical WSN sensor is often required to perform multiple functions, such as sensing, processing, and data reception and transmission, with a limited available power source. The past few years have also witnessed a growing demand for self-powered wearables that can enable vigilant health monitoring with 24/7 operation [2]–[4]. In all these applications, batteries are often undesirable due to their limited lifetime and cost, as well as their bulkiness.

For powering wearables, different modalities have been proposed and employed to harvest energy from human body [5]–[7], such as motion (mechanical) [5], heat (thermal) [6], and biochemical energy (biofuel) [7]. Among these, harvesting from body motion has the potential to extract the highest available power [8]. Electromagnetic, electrostatic, and piezoelectric are three conventional methods for converting mechanical energy into usable electrical power [9]. The piezoelectric energy harvesters (PEHs) are more attractive due to their higher power density and scalability [10]–[12].

Fig. 1 shows the generic block diagram of a piezoelectric energy harvesting system. It includes a PEH modelled with its simplified electrical equivalence (electrical current  $I_P$  and parallel internal capacitance/resistance  $C_P/R_P$ ), a power-management circuit for efficient conversion of the AC signal across the PEH to a usable DC voltage across a storage capacitor  $C_{ST\ ORE}$ , and the sensor node modelled with an equivalent DC load  $R_L$  for simplicity in this paper.

Although several unidirectional PEHs in the form of a single cantilever beam have been proposed and developed in the past [10]–[16], they suffer from several challenges in energy harvesting from body motion, including the presence of multi-axial motion, irregular frequencies, and unpredictable voltage levels with often low amplitudes [8]. To address these challenges, our team at Penn State and University of Utah has recently developed wrist-worn eccentric rotor-based inertial PEHs specifically for energy harvesting from body motion, as shown in Fig. 2 [8]. These PEHs utilize multiple magnetically or mechanically plucked flexible thin-film lead zirconate titanate (PZT)/nickel (Ni)/PZT beams to significantly increase harvested

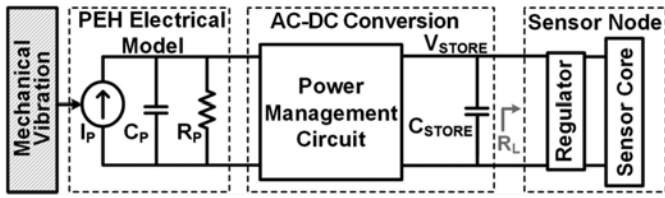


Fig. 1. Generic block diagram of a piezoelectric energy harvesting system. A power-management circuit is used to convert the AC voltage across the PEH to a usable DC voltage across a storage capacitor  $C_{STORE}$ . For simplicity, the sensor node has been modeled with a DC load  $R_L$  in this paper.

energy within a small volume. These multi-beam PEHs convert multi-axial body motion into AC voltages with different phases and shock-like decaying amplitudes (up to several volts) within the frequency range of 90–160 Hz (magnetic plucking) and 230–270 Hz (mechanical plucking) across each beam [8].

State-of-the-art power-management schemes and chips for PEH interfacing utilize full-wave active rectifier (FAR) [17], synchronized switch harvesting on inductor (SSHI) [18], energy investment [19], synchronous electrical charge extraction (SECE) [20]–[22], and sense-and-set (SaS) [23] methods. However, they suffer from multiple shortcomings: 1) they can only interface with one beam, 2) SSHI and SECE inherently suffer from large power loss in harvesting shock responses and large inputs, respectively, 3) SECE with passive negative voltage converters (NVCs) cannot harvest low PEH voltages, which often occur from body motion, and 4) the SaS circuit cannot tolerate frequency variations since its operation depends on predetermined timings and its input is limited to the CMOS voltage limit. Therefore, none of these techniques are optimal for interfacing with the multi-beam inertial PEHs in Fig. 2.

In this paper, we propose a new power-management scheme with either voltage-mode or SECE (VM-SECE) operation as well as its chip for the inertial PEHs in Fig. 2. The VM-SECE chip achieves the unique capabilities of 1) simultaneously harvesting energy from up to 6 piezoelectric beams in a modular fashion using a single shared off-chip inductor, 2) seamlessly reconfiguring itself between operating as an efficient FAR (voltage mode, VM) or SECE (i.e., reconfigurable VM-SECE) to improve the overall efficiency, extract maximum energy, and protect the chip against large inputs, eliminating the need for off-chip components as in [20] or high-voltage processes as in [21], 3) extending the input-voltage range to as low as 35 mV by utilizing active NVCs, 4) adaptive SECE operation (peak and time zero-crossing detection) to dynamically compensate for the variations of beams' electrical impedance, voltage, and frequency, and 5) optimal cold start (self-starting) with an active voltage doubler with a small footprint.

In our recent ISSCC paper [24], we briefly discussed the operation of the chip with some benchtop measurement results using the magnetically plucked PEH in Fig. 2a. In this paper, we have included the design of a more robust mechanically plucked PEH in Fig. 2b, the theoretical modeling of the reconfigurable VM-SECE scheme, a detailed description of the chip operation

and its circuit blocks, and extensive measurement results with both a commercial single-beam PEH and the custom mechanically plucked multi-beam PEH (Fig. 2b) on a robotic swing arm to mimic the mechanical excitation under pseudo walking conditions.

The multi-beam wrist-worn PEHs will be discussed in Section II, followed by the VM-SECE operation and modeling in Section III. The proposed chip architecture and circuit design will be described in Section IV, followed by the measurement setups and results in Section V and the concluding remarks in Section VI.

## II. WRIST-WORN MULTI-BEAM INERTIAL PIEZOELECTRIC ENERGY HARVESTER (PEH)

Conventional translational PEHs are designed to be unidirectional, while human motion contains a high amount of multi-axial movements [8]. In addition, human motion is typically at low and irregular frequencies (~1 Hz) [25] and, therefore, resonant PEHs operating at much higher frequencies cannot directly benefit from peak dynamic magnification. In contrast, our eccentric rotor-based rotational design uses a rotor to excite higher-frequency resonance in beams via a low-frequency motion, as a rotor does not have direction or motion limits. The rotor can also enable multi-beam excitation [8]. Fig. 2a and 2b shows wrist-worn multi-beam PEHs based on this design with magnetic and mechanical plucking, respectively. Custom fabricated bimorph PZT/Ni/PZT thin-film (60  $\mu\text{m}$  in thickness) beams are used to combine flexibility with strong piezoelectric response. Multi-beam design is implemented to achieve higher power density [26].

In Fig. 2a, the beams are magnetically plucked by placing a small magnet on the tip of each beam. The PZT beams are magnetically deflected and ring down at their natural frequency to achieve contactless actuation. Such non-contact frequency up-conversion via magnetic plucking is a promising solution. However, this technique faces several challenges. 1) The large mass at the end of a very flexible beam presents a failure risk in the presence of shocks. 2) the magnetic interaction between the two permanent magnets (placed at the beam tip and on the rotor) creates a detent torque on the rotor as it tries to move past the beam. Therefore, there exists a critical excitation strength below which the harvested power is negligibly small. And 3) the assembly of the electrical connections is constrained to a minimal area near the center of the device, which has led to low yield and unreliable electrical connections. This PEH was used in our prior work for interfacing with our VM-SECE chip [24].

To overcome these issues, we recently developed a similar device with mechanical plucking, as shown in Fig. 2b. The beams are excited by the pins on the rotor. This redesign removes the need for large inertia (i.e., magnet mass) at the end of the beam. This arrangement enables us to re-orient the beams such that the free end of the beam is at the center rather than the perimeter of the device, allowing us to use more standard electrical connectors and greatly simplify the device assembly. Furthermore, re-orienting the beams reduces the detent torque, which is proportional to the lever arm between the center of

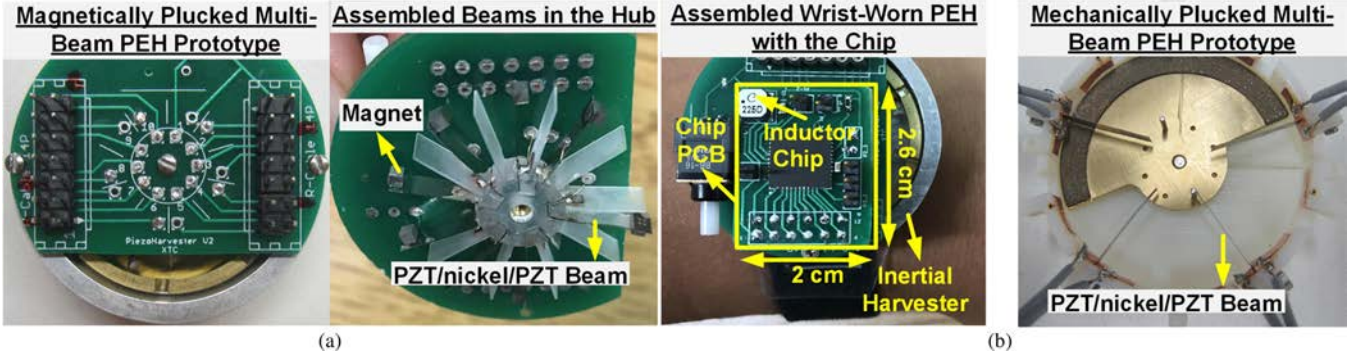


Fig. 2. Wrist-worn multi-beam piezoelectric energy harvesters (PEHs) for harvesting energy from body motion with multi-axial movements. (a) The magnetic-plucking prototype used in our previous work in [24]. (b) The mechanical-plucking prototype with more robustness used in this paper.

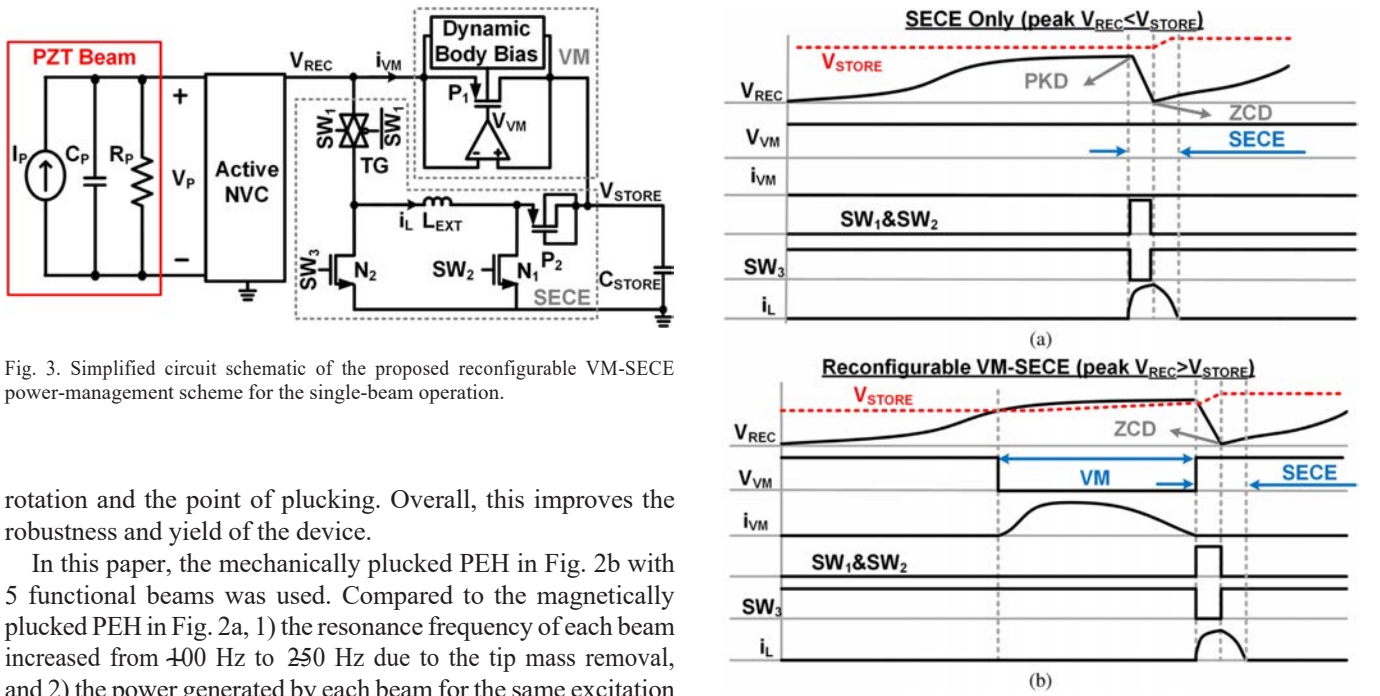


Fig. 3. Simplified circuit schematic of the proposed reconfigurable VM-SECE power-management scheme for the single-beam operation.

rotation and the point of plucking. Overall, this improves the robustness and yield of the device.

In this paper, the mechanically plucked PEH in Fig. 2b with 5 functional beams was used. Compared to the magnetically plucked PEH in Fig. 2a, 1) the resonance frequency of each beam increased from 400 Hz to 250 Hz due to the tip mass removal, and 2) the power generated by each beam for the same excitation was reduced because the pins on the rotor barely impact the PZT beams, reducing the beams displacement amplitude (i.e., a tradeoff between robustness and power generation).

### III. OPERATION AND MODELING OF THE VM-SECE SCHEME

Fig. 3 shows the simplified circuit schematic of the proposed reconfigurable VM-SECE scheme for the single-beam operation. It includes an active NVC followed by an active voltage rectifier (creating a FAR for VM operation) and a conventional SECE circuit in parallel to charge  $C_{STORE}$  to  $V_{STORE}$ . The voltage across the beam ( $V_P$ ) is first full-wave rectified by the active NVC, generating  $V_{REC}$ . As long as peak  $V_{REC} < V_{STORE}$ , the active rectifier is off ( $P_1$ : OFF), and  $C_P$  is charged by  $I_P$  to operate the circuit in the SECE mode. When peak  $V_{REC} > V_{STORE}$ , the active rectifier turns on and the circuit seamlessly transitions from VM to SECE operation.

Fig. 4a shows key operational waveforms of the VM-SECE scheme in only conventional SECE mode (peak  $V_{REC} <$

Fig. 4. Key operational waveforms of the proposed VM-SECE scheme. (a) SECE only when peak  $V_{REC} < V_{STORE}$ . (b) Reconfigurable VM-SECE when peak  $V_{REC} > V_{STORE}$ .

$V_{STORE}$ ).  $I_P$  first charges  $C_P$  until  $V_{REC}$  reaches its peak detected by a peak-detection circuit (PKD). Then at  $V_{REC}$  peak, when maximum energy is stored in  $C_P$ ,  $C_P$  energy is transferred to an external inductor  $L_{EXT}$  for a short time period via enabling  $SW_1$  (transmission gate  $TG$ : ON) and  $SW_2$  ( $N_1$ : ON) and disabling  $SW_3$  ( $N_2$ : OFF) until  $V_{REC}$  reduces to zero, which is detected by a time zero-crossing detection (ZCD) circuit. Then  $L_{EXT}$  energy is transferred to  $C_{STORE}$  via a diode (diode-connected  $P_2$ ) by disabling  $SW_1$  and  $SW_2$  ( $TG$ ,  $N_1$ : OFF), and enabling  $SW_3$  ( $N_2$ : ON).

In the SECE mode (Fig. 4a), the energy stored in  $C_P$  at peak  $V_{REC}$  is given by,

$$E_{SECE-only} = \frac{1}{2} C_P (2V_{P,OC})^2 = 2C_P V_{P,OC}^2, \quad (1)$$

where  $V_{P,OC}$  is the  $V_P$  peak when the PEH is not loaded (PEH open circuit voltage). The  $V_P$  peak in (1) is  $2V_{P,OC}$  because in the SECE mode  $C_P$  is discharged by  $L_{EXT}$  instead of  $I_P$ . In other words, SECE-only operation imposes very high voltages on the PEH and the interface circuit. Due to the full-wave rectification, the frequency of energy extraction is twice higher than the PEH excitation frequency  $f_P$ . Therefore, the stored power in SECE-only mode can be calculated as,

$$P_{STORE,SECE-only} = 2f_P E_{SECE-only} = 4C_P V_{P,OC}^2 f_P. \quad (2)$$

Fig. 4b shows the key operational waveforms in the VM-SECE mode (peak  $V_{REC} > V_{STORE}$ ). When  $V_{REC}$  slightly surpasses  $V_{STORE}$ ,  $P_1$  turns on and charges  $C_{STORE}$  with high efficiency via  $I_P$  (VM path) until  $I_P$  reaches zero. This is similar to a FAR operation. As  $V_{REC}$  goes slightly below  $V_{STORE}$ ,  $P_1$  is turned off, and the SECE circuit is triggered to extract the remaining stored energy in  $C_P$  as explained before in Fig. 4a. Therefore, peak  $V_P$  always stays close to  $V_{STORE}$ .

The output power of the FAR can be found from [27],

$$P_{STORE,FAR} = 2f_P C_P V_{STORE} [2V_{P,OC} - (V_F - V_I)], \quad (3)$$

where  $V_F$  and  $V_I$  are the final and initial voltages of  $V_P$  (input) in a half cycle, respectively. For the FAR,  $V_I = V_{STORE}$  and  $V_F = V_{STORE}$  and, therefore, the stored power can be found from,

$$P_{STORE,FAR} = 4f_P C_P V_{STORE} [V_{P,OC} - V_{STORE}], \quad (4)$$

The VM operation is also similar to the FAR operation but due to the SECE operation following VM in Fig. 4b,  $C_P$  is charged by  $I_P$  only from 0 to  $V_{STORE}$ , i.e.,  $V_I = 0$  and  $V_F = V_{STORE}$ . Therefore, the output power obtained by the VM operation can be calculated as,

$$P_{STORE,VM} = 2f_P C_P V_{STORE} [2V_{P,OC} - V_{STORE}]. \quad (5)$$

Right after the VM operation, the remaining energy in  $C_P$  ( $V_P < V_{STORE}$ ) is extracted by SECE and, therefore, the stored power in this time period can be calculated from,

$$P_{STORE,SECE} = \frac{1}{2} C_P V_{STORE}^2 (2f_P) = C_P V_{STORE}^2 f_P. \quad (6)$$

Finally, using (5) and (6) the total stored power during the VM-SECE operation can be calculated as,

$$\begin{aligned} P_{STORE,VM-SECE} &= P_{STORE,VM} + P_{STORE,SECE} \\ &= f_P C_P V_{STORE} [4V_{P,OC} - V_{STORE}]. \end{aligned} \quad (7)$$

The damping loss ( $R_P$ ) is neglected in all these equations.

Fig. 5a and 5b shows the simulated and calculated  $P_{STORE}$  and simulated peak  $V_{REC}$  vs.  $V_{STORE}$ , respectively, for the FAR, conventional SECE and proposed VM-SECE scheme under ideal lossless condition with  $C_P = 10$  nF,  $R_P = \infty$ ,  $L_{EXT} = 2.2$  mH,  $V_{P,OC} = 4.71$  V, and  $f_P = 100$  Hz. For  $P_{STORE}$  calculations, (2), (4), and (7) were used for the conventional SECE, FAR, and VM-SECE, respectively. For simulations, the circuits were built in the Cadence Spectre circuit

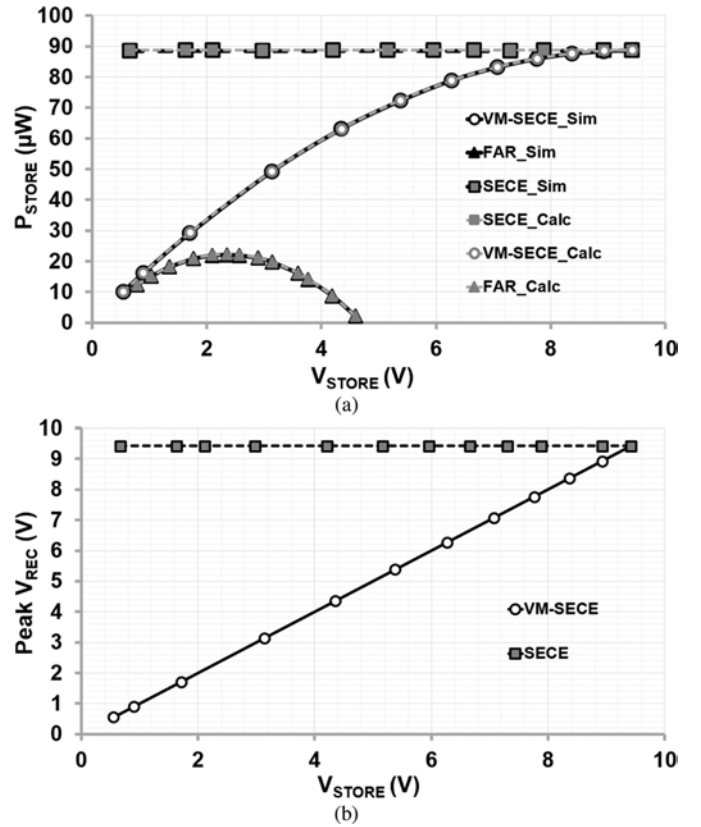


Fig. 5. (a) Simulated and calculated  $P_{STORE}$  vs.  $V_{STORE}$  for the FAR, conventional SECE and the proposed VM-SECE. (b) Simulated peak  $V_{REC}$  vs.  $V_{STORE}$  for the proposed VM-SECE and conventional SECE. Ideal lossless components were used in both calculations and circuit simulations.

simulator (Cadence Technology, San Jose, CA, USA) with ideal components.

Three lessons can be learned from Fig. 5a. 1) The obtained  $P_{STORE}$  by VM-SECE and FAR are close at low  $V_{STORE} < 2$  V because a negligible amount of energy is wasted in charging  $C_P$ . As  $V_{STORE}$  increases, more energy is wasted with FAR operation while VM-SECE can extract all the remaining energy inside  $C_P$  via the SECE operation. 2) When  $V_{STORE} > 2V_{P,OC} = 9.42$  V, the VM-SECE scheme reconfigures itself to the SECE mode providing the same  $P_{STORE}$  as in conventional SECE. Nonetheless, for  $V_{STORE} < 9.42$  V conventional SECE achieves higher  $P_{STORE}$  with ideal components. And 3) the calculation and simulation results match very well, validating the accuracy of our models.

Although the conventional SECE achieves higher  $P_{STORE}$  for most  $V_{STORE}$  values with ideal components (Fig. 5a), as shown in Fig. 5b the peak  $V_{REC}$  in conventional SECE is significantly high (9.42 V in these simulations) for all  $V_{STORE}$  values. However, employing VM operation in the VM-SECE scheme limits the peak  $V_{REC}$  to  $V_{STORE}$  providing inherent and efficient over-voltage protection (OVP) and eliminating the need for circuit implementation in high-voltage processes.

To provide a fair comparison between conventional SECE and the proposed VM-SECE with lossy components, circuit simulations were done for these circuits (Fig. 3) with the circuit

TABLE I  
CIRCUIT PARAMETERS USED FOR VM-SECE AND SECE SIMULATIONS

Parameters	Value	Transistors	Size (W/L)
$C_P$ (nF)	10	$P_1$	20 $\mu\text{m}/0.5\mu\text{m}$
$R_P$ (M $\Omega$ )	1	$P_2$	2000 $\mu\text{m}/0.5\mu\text{m}$
$L_{EXT}$ (mH)/Series Ohmic Loss ( $\Omega$ )	2.2 / 11	$N_1$	1200 $\mu\text{m}/0.5\mu\text{m}$
$V_{P,OC}$ (V)	2.67	$N_2$	1200 $\mu\text{m}/0.5\mu\text{m}$
$f_P$ (Hz)	100	TG	P 1200 $\mu\text{m}/0.5\mu\text{m}$
$V_{DD}$ (V)	3		N 1200 $\mu\text{m}/0.5\mu\text{m}$

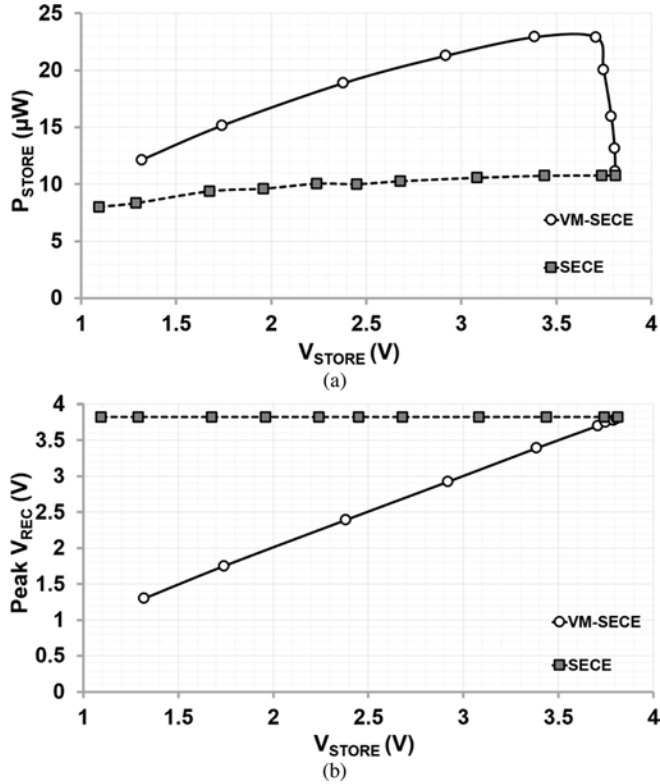


Fig. 6. Simulated (a)  $P_{STORE}$  and (b) peak  $V_{REC}$  vs.  $V_{STORE}$  for the proposed VM-SECE scheme and the conventional SECE with lossy circuit components listed in Table I. The circuit schematic is shown in Fig. 3.

parameters listed in Table I (transistors in a 0.35  $\mu\text{m}$  CMOS process) for  $V_{P,OC} = 2.67$  V at the supply voltage  $V_{DD}$  of 3 V. Fig. 6a and 6b shows the simulated  $P_{STORE}$  and peak  $V_{REC}$  vs.  $V_{STORE}$ , respectively, for the proposed VM-SECE and conventional SECE using lossy components listed in Table I. It can be seen that the VM-SECE scheme outperforms the conventional SECE for all  $V_{STORE}$  values in terms of achieving higher  $P_{STORE}$  with much lower  $V_{REC}$  until  $V_{STORE} \approx 3.8$  V. In these simulations, the VM-SECE performance degrades at  $V_{STORE} \approx 3.8$  V because the PMOS transistor of TG in Fig. 3 starts to leak as  $V_{REC}$  increases above  $V_{DD} = 3$  V by a threshold voltage of 0.8 V. Nonetheless, the simulation results in Fig. 6 shows the advantage of the proposed VM-SECE scheme compared to conventional SECE in providing both higher  $P_{STORE}$  and inherent OVP.

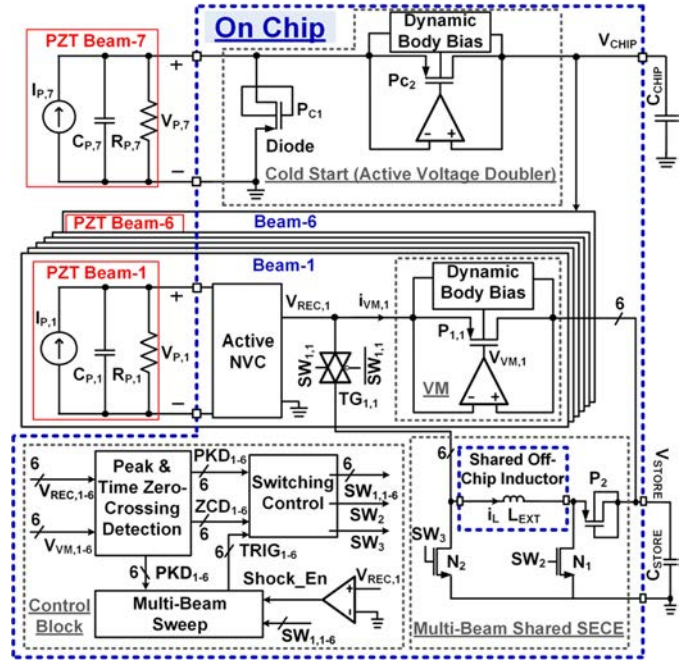


Fig. 7. Block diagram of the proposed multi-beam shared-inductor reconfigurable VM-SECE chip with cold start.

#### IV. MULTI-BEAM RECONFIGURABLE VM-SECE CHIP ARCHITECTURE

Fig. 7 shows the block diagram of the proposed chip. It includes 1) six identical active rectifiers with active NVCs (FAR for VM path: one per beam) connected in parallel to allow simultaneous VM operation (due to the low-frequency operation, the reverse current is negligible and, therefore, low-power comparators without offset compensation have been designed), 2) a shared SECE circuit for all six beams to reduce the number of off-chip inductors from six to one, 3) a control block for optimal switching in different modes, and 4) a voltage doubler interfaced to an additional 7th beam for optimal cold start. The chip externally requires one inductor  $L_{EXT}$ , one storage capacitor  $C_{STORE}$ , and one cold-start capacitor  $C_{CHIP}$ , which with  $C_{P,7}$  forms a voltage doubler (eliminating one external capacitor; small footprint) to supply the chip's internal circuitry via  $V_{CHIP}$ . As shown in Fig. 7, a conventional dynamic body-bias circuit with two PMOS transistors (similar to [28]) in both active rectifiers and voltage doubler connects the bulk of the PMOS pass transistors to the highest potential between their source and drain, removing undesired currents.

Fig. 8a shows the key waveforms of the VM-SECE chip for asynchronous inputs, which is the case for the inertial PEHs in Fig. 2. The chip does VM operation automatically and simultaneously for all beams in parallel. It also sweeps the beams one by one every 60  $\mu\text{s}$  to check their  $V_P$  for generating optimal switching signals for the SECE operation whenever the condition is met as described in Fig. 4 (either  $V_{REC}$  reaches its peak without VM operation or at the end of VM operation). Fig. 8b shows similar waveforms for synchronous inputs (worst-case scenario), in which the shared SECE circuit is time multiplexed

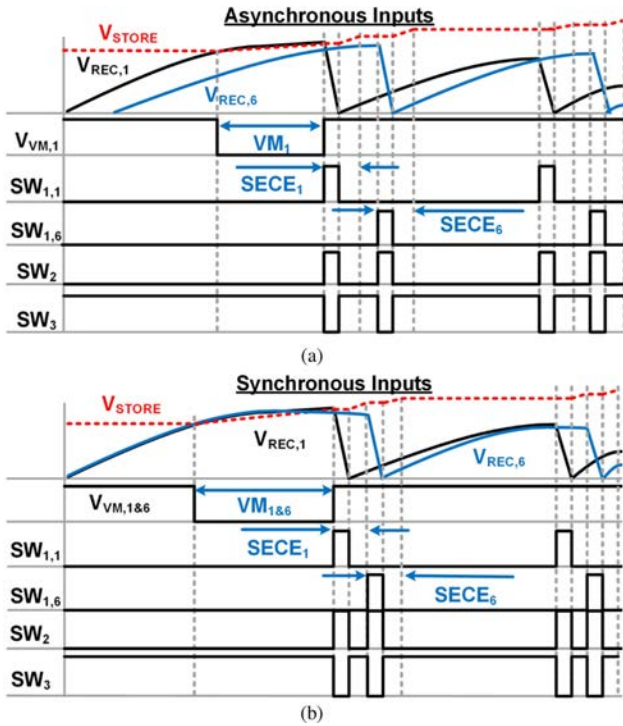


Fig. 8. Key operational waveforms of the proposed VM-SECE chip for (a) asynchronous and (b) synchronous inputs (beams 1 and 6 in this example).

between beams. This is possible with minimal loss because full SECE operation requires only  $50 \mu\text{s}$ , which is much faster than the low-frequency inputs.

Fig. 9 shows schematic diagrams of active NVC and control block including multi-beam sweep, peak and time zero-crossing detection (PKD & ZCD), and switching control circuits. In the NVC in Fig. 9a, a comparator switches pass transistors to actively full-wave rectify the input ( $V_{P,n}$ ;  $n = 1-6$ ) with minimal voltage drop.

In the multi-beam sweep circuit in Fig. 9b, beams' voltages ( $V_{P,n}$ ) are checked one by one every  $60 \mu\text{s}$  in a loop by 6 cascaded beam-control blocks. There are 4 possible conditions: 1)  $C_{P,n}$  is charging and  $V_{REC,n} < V_{ST ORE}$ , 2)  $C_{ST ORE}$  is charging via VM and  $V_{REC,n} > V_{ST ORE}$ , 3) VM operation ended ( $V_{VM,n}$  in Fig. 7 is high) with some charges left on  $C_{P,n}$ , and 4)  $V_{REC,n}$  reaches its peak and is still smaller than  $V_{ST ORE}$ . Under conditions one and two ( $PKD_n$  in Fig. 7 is low), beam- $n$  is skipped through the flip-flop  $FF_{2,n}$  followed by  $60 \mu\text{s}$  delay to check the next beam. Under conditions three and four ( $PKD_n$ : high), at which SECE should immediately start, the beam control waits until SECE operation ends ( $SW_{1,n}$  goes low) to clock  $FF_{1,n}$  and trigger the next beam after  $60 \mu\text{s}$ .

Fig. 9c shows the PKD & ZCD circuit [20]. A positive edge is generated at  $V_{REC,n}$  peak and combined with  $V_{VM,n}$  to clock a flip-flop for generating high  $PKD_n$  (indicating start of SECE), which is reset to low at  $V_{REC,n} = 0$ , detected by time zero-crossing ( $ZCD_n$ : high). Finally, Fig. 9d shows the switching control that generates required six  $SW_{1,n}$ ,  $SW_2$  and  $SW_3$  signals based on the waveforms in Figs. 4 and 8.

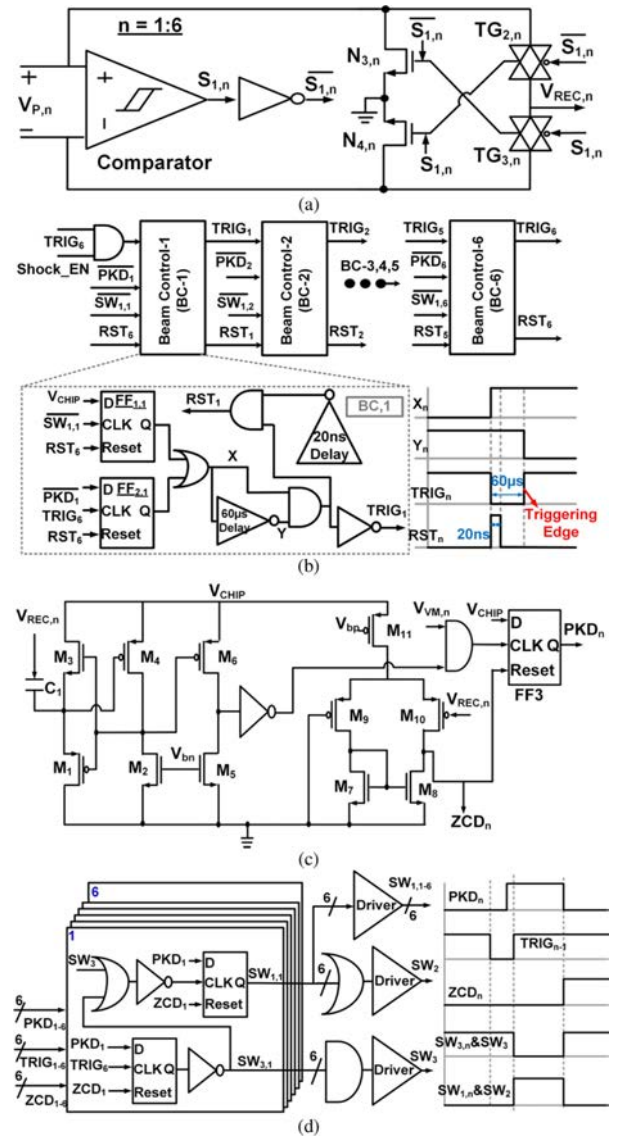


Fig. 9. Detailed schematic diagrams of the (a) NVC, (b) multi-beam sweep control, (c) peak and time zero-crossing detection, and (d) switch control.

## V. MEASUREMENT RESULTS

A proof-of-concept VM-SECE chip was fabricated in a  $0.35\text{-}\mu\text{m}$  2P4M standard CMOS process, occupying  $1.9 \text{ mm}^2$  active area (Fig. 10). The chip was extensively characterized with measurements in benchtop settings, with a commercial single-beam PEH on a shaker, and with the mechanical plucking 5-beam PEH in Fig. 2b on a robotic swing arm. In all measurements,  $L_{EXT} = 2.2 \text{ mH}$  (LPS5030-225MR, Coilcraft Inc., Cary, IL, USA) with measured dimensions of  $4.78 \text{ mm} \times 4.78 \text{ mm} \times 2.87 \text{ mm}$ ,  $C_{ST ORE} = 47 \mu\text{F}$ , and  $C_{CHIP} = 10 \mu\text{F}$  were used.

### A. Benchtop Measurements

Fig. 11 shows the measured key operational waveforms, including  $V_{REC}$ ,  $PKD$ , and  $ZCD$ , and different operation modes of the chip with one beam. Similar to theoretical waveforms in

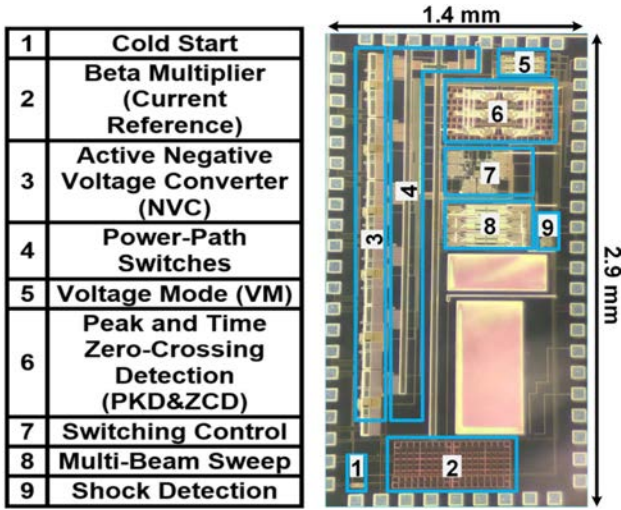


Fig. 10. The proposed VM-SECE chip micrograph occupying 1.9 mm<sup>2</sup> of active area, and its key building blocks.

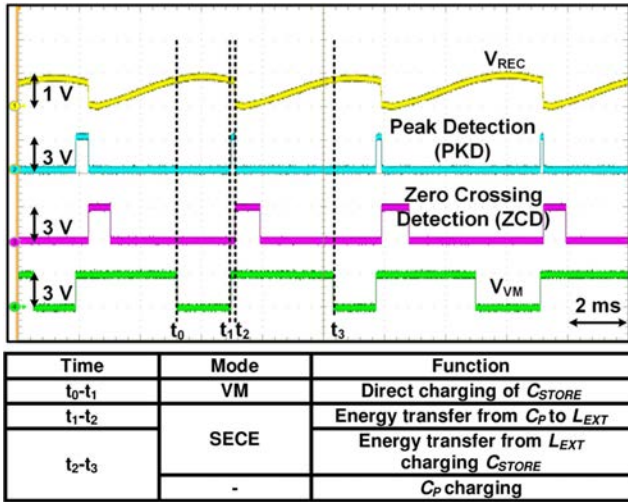


Fig. 11. Measured key operational waveforms showing the VM-SECE chip operation in different modes with one beam.

Fig. 4b, the chip properly transitioned between VM and SECE by automatically detecting  $V_{REC}$  peaks and time zero crossings.

Fig. 12 shows the chip's measured transient waveforms when the multi-beam inertial PEH was manually shaken gently. In Fig. 12a, during the cold start  $C_{CHIP}$  was first charged via  $P_{C2}$  in Fig. 7 in a passive manner to  $\sim 1.5$  V, at which the active voltage doubler started to operate and charged  $C_{CHIP}$  efficiently to  $V_{CHIP} = 3.2$  V with  $V_{P,7}$  peak-peak voltages as large as 4 V. The DC shift of  $V_{P,7}$  in Fig. 12a is due to  $C_{P,7}$  and  $P_{C1}$  in Fig. 7. Similarly for  $V_{CHIP} < 1.5$  V,  $C_{STORE}$  was charged via six  $P_{1,n}$  transistors (in VM path) in a passive manner to  $\sim 1.5$  V, at which VM active rectifiers started to operate, further charging  $C_{STORE}$  to  $\sim 1.9$  V via VM for  $V_{CHIP} < 3$  V (chip not fully functional yet). As  $V_{CHIP} > 3$  V, the chip operated in reconfigurable VM-SECE mode (fully functional) to charge  $C_{STORE}$  more efficiently (faster rate in Fig. 12a)

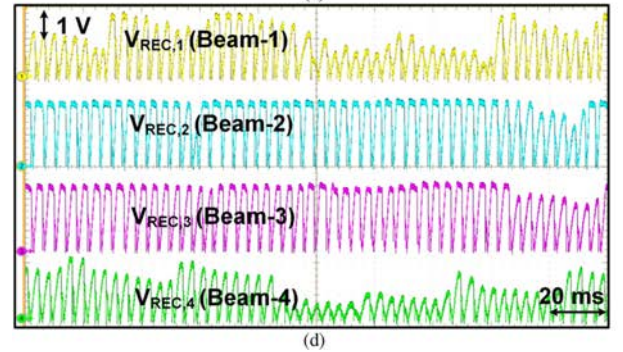
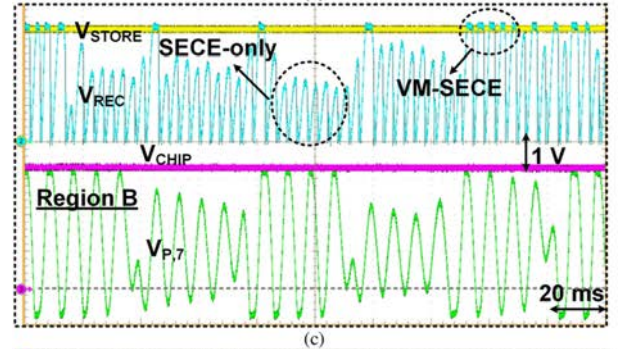
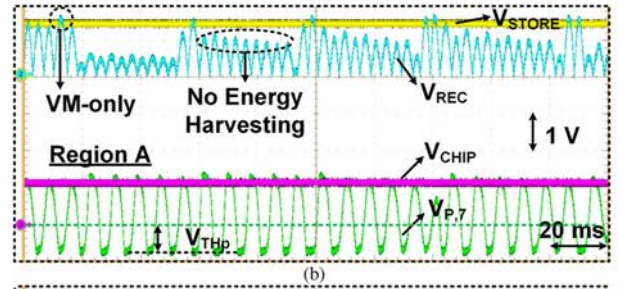
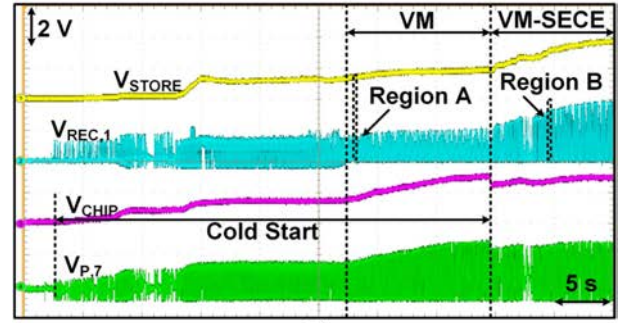


Fig. 12. Benchtop measurement results of the chip with the multi-beam PEH. (a) Measured transient waveforms with cold start. (b) and (c) Zoomed waveforms for  $V_{CHIP} < 3$  V and  $V_{CHIP} > 3$  V, respectively. (d)  $V_{REC}$  waveforms across 4 beams.

to  $V_{STORE} > 1.9$  V at the presence of different voltage and frequency variations at each beam.

Fig. 12b and 12c shows the zoomed waveforms of Fig. 12a for  $V_{CHIP} < 3$  V (region A: chip not functional yet) and  $V_{CHIP} > 3$  V (region B: chip fully functional), respectively. It can be seen in Fig. 12b that whenever peak  $V_{REC}$  surpasses  $V_{STORE}$ ,  $C_{STORE}$  was charged via the VM operation. For most cycles, there was no energy harvesting. However, when the chip was fully functional in Fig. 12c, energy was extracted from each cycle via SECE-only or VM-SECE operations. Fig. 12d shows

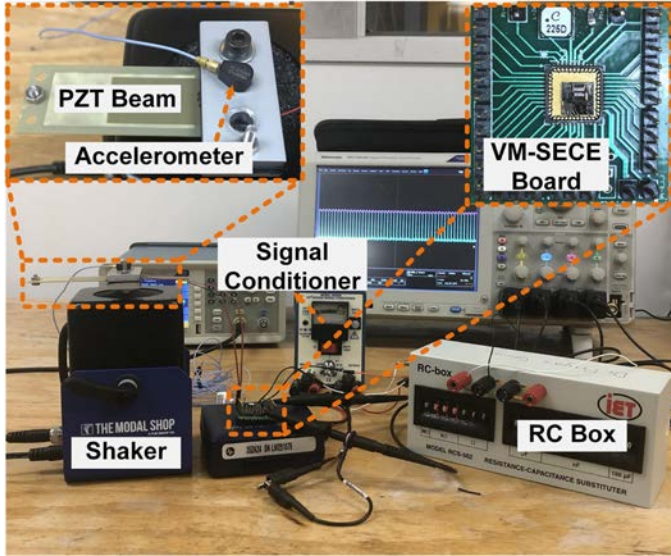


Fig. 13. Measurement setup for characterizing the chip's performance with a commercial single-beam PEH (PPA1011) on a shaker.

the rectified voltages across 4 different beams to highlight the voltage and frequency variabilities across multiple beams.

### B. Measurements With a Commercial Single-Beam PEH

To provide a fair comparison to prior arts, the performance of the VM-SECE chip was characterized with a commercial PEH with a single beam (PPA1011, MIDE Tech., Woburn, MA, USA). Fig. 13 shows the measurement setup for the PPA1011 with a 0.9-gram tip mass and resonance frequency ( $f_p$ ) of 56 Hz. A custom fabricated clamp fixed the beam on a smart shaker (K2007E01, The Modal Shop, Sharonville, OH, USA).

An accelerometer (352A24, PCB Piezoelectronics, Depew, NY, USA) connected to a signal conditioner (480E09, PCB Piezoelectronics, Depew, NY, USA) was placed on the clamp to measure the shock-input accelerations. The beam outputs were connected to the chip. An RC box (RCS-502, IET Labs, Inc, Roslyn Heights, NY, USA) provided different resistive loading ( $R_L$ ) across  $C_{STORE}$ . Shocks with different energies at the 1 Hz frequency with the optimal pulse width of 8.1 ms were applied to the smart shaker.

Fig. 14 shows the VM-SECE chip improvements of  $P_{STORE}$  at different  $V_{STORE}$  for PPA1011 shock acceleration of 4.39 g at 1 Hz resulting in  $V_{P,OC} = 2.82$  V, compared to an on-chip FAR with measured 95.6% efficiency. At  $V_{STORE} = 1.8$  V, the VM-SECE chip harvested 3.28x more power than the maximum power harvested by the FAR at  $V_{STORE} = 1$  V ( $3.7 \mu\text{W}$  vs.  $1.2 \mu\text{W}$ ). This results in a shock figure of merit (FoM) of 328%, which is defined as the ratio of the maximum harvested energy by the chip to that of a full-wave rectifier [21]. Overall, the VM-SECE chip achieved much higher  $P_{STORE}$  for a wide range of  $V_{STORE}$ .

Fig. 15 shows the measured FoM and  $V_{P,OC}$  vs. different shock accelerations of the PPA1011 PEH at 1 Hz. Under various shock accelerations, the VM-SECE chip maintained a high FoM

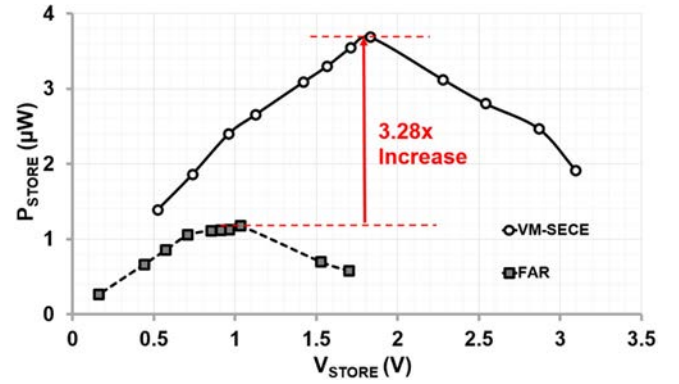


Fig. 14. Comparison of measured  $P_{STORE}$  vs.  $V_{STORE}$  between the VM-SECE chip and the on-chip 95.6%-efficient FAR using the commercial PPA1011 PEH (single beam) with the shock acceleration of 4.39 g at 1 Hz.

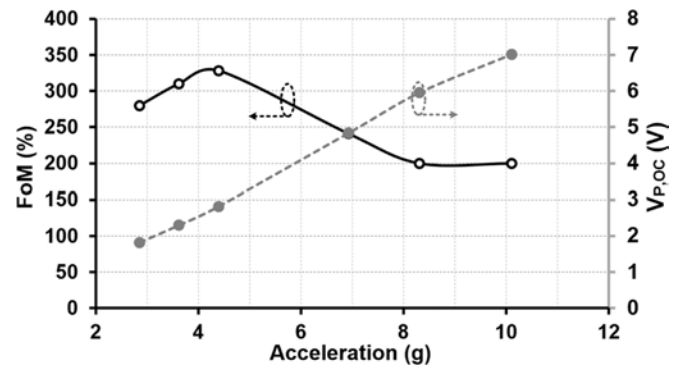


Fig. 15. Measured FoM and  $V_{P,OC}$  of the VM-SECE chip under various shock accelerations. A minimum FoM of 200% was achieved.

of  $> 200\%$  ( $>2x$  improvement in  $P_{STORE}$  compared to the on-chip FAR). As the shock acceleration increased  $> 4.5$  g, the FoM reduced because the VM-SECE chip supply was 3 V and leakage current increased for  $V_{STORE} > 3.8$  V as discussed in Section III. As the shock acceleration increased from 2.85 g to 10.1 g, the  $V_{P,OC}$  increased from 1.8 V to 7 V as shown in Fig. 15.

### C. Measurements With the Custom Multi-Beam PEH

To verify the functionality of the proposed VM-SECE chip in a more realistic setup (similar to wearables), the chip was integrated with the mechanically plucked 5-beam PEH in Fig. 2b and tested on a robotic swing arm (one input of the chip was left open) [8]. Fig. 16 shows the measurement setup with a motor-controlled swing arm replicating a pseudo-walking motion. The 50 cm long aluminum arm roughly mimics the human upper limb. The micro-stepping-enabled stepper motor was programmed to create varying motion profiles in a sinusoidal fashion with 25 degrees of rotation amplitude and 0.8-second period (fast pseudo walking) [8].

Fig. 17 shows the measured transient waveforms of the rectified voltage of three beams ( $V_{REC1,2,3}$ ) and  $V_{STORE}$ . As the arm started swinging,  $C_{STORE}$  was charged to  $V_{STORE} \approx 2$  V with first VM and then reconfigurable VM-SECE operation



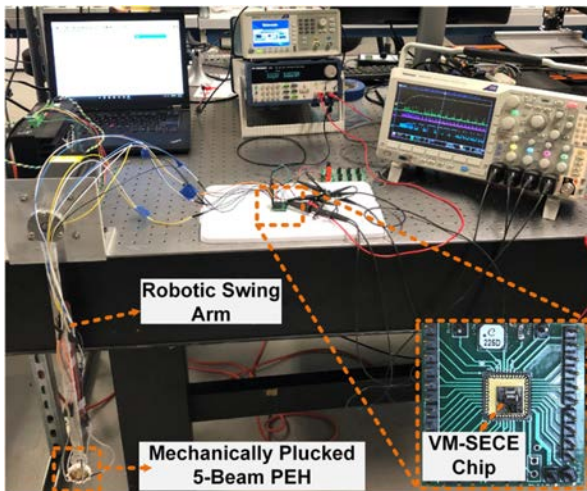


Fig. 16. Measurement setup with the integrated VM-SECE chip and 5-beam mechanically plucked PEH (Fig. 2b) mounted on a robotic swing arm.

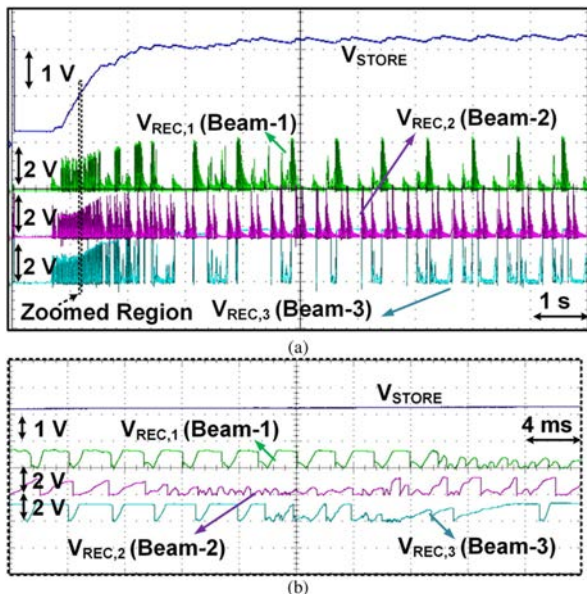


Fig. 17. (a) Measured transient voltage waveforms of the VM-SECE chip interfacing the 5-beam mechanically plucked PEH in Fig. 2b on the robotic swing arm. (b) Zoomed waveforms showing voltage variability across beams.

within  $\sim 10$  sec as shown in Fig. 17a. The zoomed waveforms in Fig. 17b show the variability of the voltage across different beams. Almost 4 s after the chip startup, the circuit operation ( $V_{STORE}$ ) reached its steady state as shown in Fig. 17a.

Fig. 18a and 18b compares measured  $P_{STORE}$  at different  $V_{STORE}$  values of the VM-SECE chip and the on-chip FAR for operation with one and five beams on the robotic swing arm, respectively. The VM-SECE chip harvested 1.59x (FoM = 159%) and 2.38x (FoM = 238%) more power than the maximum energy harvested using the FAR for 1- and 5-beam operation, respectively. Utilizing 5 beams further enhanced the FoM because the VM-SECE scheme extracted almost all energy

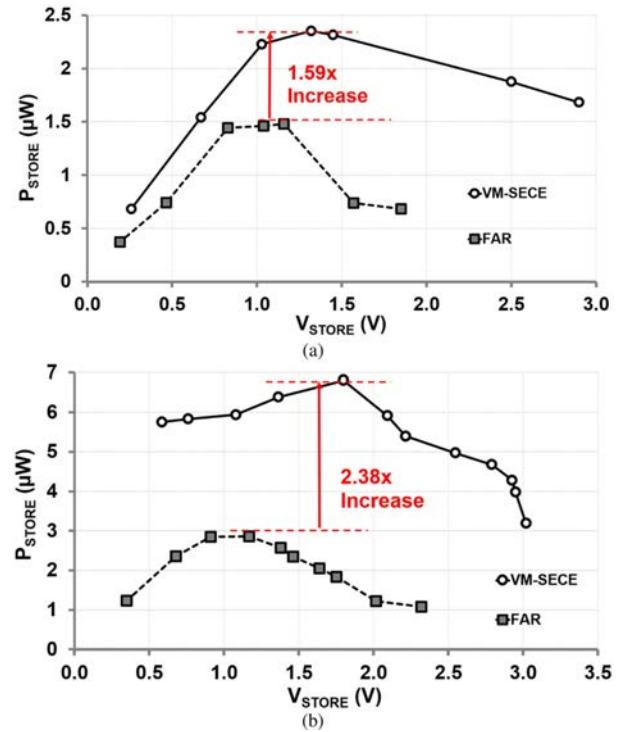


Fig. 18. Comparison of measured  $P_{STORE}$  vs.  $V_{STORE}$  between the VM-SECE chip and the on-chip FAR using the custom PEH in Fig. 2b on the robotic swing arm. (a) One-beam operation. (b) Five-beam operation.

from individual beams regardless of their voltage levels but 5 parallel FARs could not.

Table II benchmarks the VM-SECE chip against state-of-the-art PEH chips. To the best of our knowledge, the VM-SECE chip offers the first integrated solution that can harvest from up to 6 beams simultaneously in a modular fashion, with inputs as low as 35 mV, which makes it suitable for energy harvesting from multi-axial body motion. It can reconfigure itself between VM and SECE to improve the overall efficiency, extract maximum power, and protect itself from high voltages. With a commercial single-beam PEH, our VM-SECE chip achieved a high FoM of 328% at  $V_{P,OC} = 2.8$  V compared to an on-chip FAR with 95.6% efficiency. The slightly higher FoM of 330% in [21] with a SECE interface is mainly due to their FoM calculation with a passive rectifier, which is less efficient than a FAR. Also, a high-voltage (10 V) process is used in [21]. With our custom 5-beam mechanically plucked PEH, our VM-SECE chip achieved an FoM of 238% at  $V_{P,OC} = 5$  V.

As listed in Table II, the VM-SECE chip achieved highest end-to-end measured efficiencies of 95.6% and 84.6% at  $P_{STORE}$  of 8.5  $\mu$ W and 10.2  $\mu$ W for VM and VM-SECE operation, respectively. Conventional input power measurement using a current-sensing resistor was used to measure the efficiency in VM. The same method could not accurately be used for the VM-SECE, because the input current in VM and SECE were significantly different. Therefore, to measure the VM-SECE efficiency, the maximum extracted powers ( $P_{STORE}$ ) for only a single beam (no chip) and the VM-SECE chip both interfaced with optimal resistive loads were measured for the same input

TABLE II  
BENCHMARKING THE PROPOSED 6-BEAM RECONFIGURABLE VM-SECE CHIP AMONG THE STATE-OF-THE-ART PEH CHIPS

Publication	ISSCC 2016, [18]	ISSCC 2013, [19]	JSSC 2014, [20]	JSSC 2018, [21]	ISSCC 2019, [23]	ISSCC 2019, [24] (Our Work)	This Work	
CMOS Tech (nm)	350	350	350	40 (HV 10 V)	0.18	350	350	
Chip Size (mm <sup>2</sup> )	0.72	2.34	3.6	0.55	0.47	1.9	1.9	
Scheme Type	SSHI	Energy Investment	Multi-Shot SECE	SECE	SaS	Reconfigurable VM-SECE	Reconfigurable VM-SECE	
# of Beams (Chip Inputs)	1	1	1	1	1	6 (Modular)	6 (Modular)	
Piezoelectric Energy Harvester (PEH)	MIDE V21B & V22B	MIDE V22B	Murata	MIDE PPA1011	MIDE PPA1022	*6-Beam Magnetically Plucked Custom PZT/Nickel/ PZT	Single-Beam MIDE PPA1011	*5-Beam Mechanically Plucked Custom PZT/Nickel/ PZT
C <sub>p</sub> (nF)	26	15	23	100	8	17 - 49	100	15 - 20
Beam Dimensions l×w×t (mm)	6.25 × 1.5 × 0.7	6.25 × 1.5 × 0.7	-	71 × 25.4 × 0.7	53 × 10.3 × 0.74	12 × 3 × 0.06 (each beam, flexible)	71 × 25.4 × 0.7	19.5 × 3 × 0.062 (each beam, flexible)
Excitation Type	Periodic & Shock	Periodic	Periodic	Periodic & Shock	Periodic & Shock	Multi-Axial Body Motion	Shock	Multi-Axial Body Motion
Operation Freq. (Hz)	225	143	100	75.4	85	90 - 160	60	230 - 270
FoM* (%) @ V <sub>F,OC</sub> (V)	269 @ 2.5	-	-	330** @ 3.4	316 @ 0.95 325 @ 0.4	1-Beam: 365 @ 1.6 6-Beam: 511 @ 1.6	328 @ 2.8	1-Beam: 159 @ 5 5-Beam: 238 @ 5
Cold Startup	Yes	No	Yes	Yes	No	Yes	Yes	
Maximum End-to-end Efficiency (%) @ P <sub>STORE</sub> (μW)	~88**	69.2	61	94	-	VM: 95.6 @ 8.5 VM-SECE: 84.6 @ 10.2	VM: 95.6 @ 8.5 VM-SECE: 84.6 @ 10.2	
Minimum Input (mV)	670	570	-	-	-	35	35	
Quiescent Current (μA)	1	0.1	0.3	0.03	-	0.5 (6 beams)	0.5 (6 beams)	

\*FoM = Max (P<sub>store</sub>)/Max (P<sub>FAR</sub>) for shock input (FAR: Full-wave Active Rectifier).

\*Wrist-worn PEH.

\*\*Calculated from the paper.

\*\*Instead of an active rectifier, a passive rectifier was used.

excitation. It should be noted that this leads to an optimistic value for the VM-SECE efficiency.

## VI. CONCLUSION

We have presented the theory, implementation, and comprehensive measurement results of a fully autonomous multi-beam reconfigurable VM-SECE chip with only one shared off-chip inductor for inertial energy harvesting, particularly from multi-axial body motion. Despite drastic variability of voltage across different beams as well as their frequency variations, the VM-SECE chip could harvest energy from up to 6 beams simultaneously in a modular fashion with improved efficiency and energy extraction, as well as inherent OVP. When interfaced with a commercial single-beam PEH, the chip could extract 3.28x more power compared to the best of an active rectifier with 95.6% efficiency. Experimental results with a custom-made mechanically plucked 5-beam inertial PEH mounted on a robotic swing arm, mimicking pseudo-walking, showed that the VM-SECE chip can operate properly in charging a storage capacitor and achieves a high FoM of 238%. Our proposed multi-beam inertial PEH and VM-SECE chip hold the promise of integrated self-powered solutions for the next generation of wearables with vigilant operation capability.

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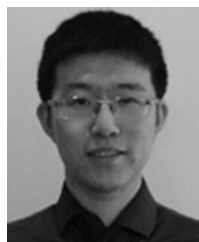


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