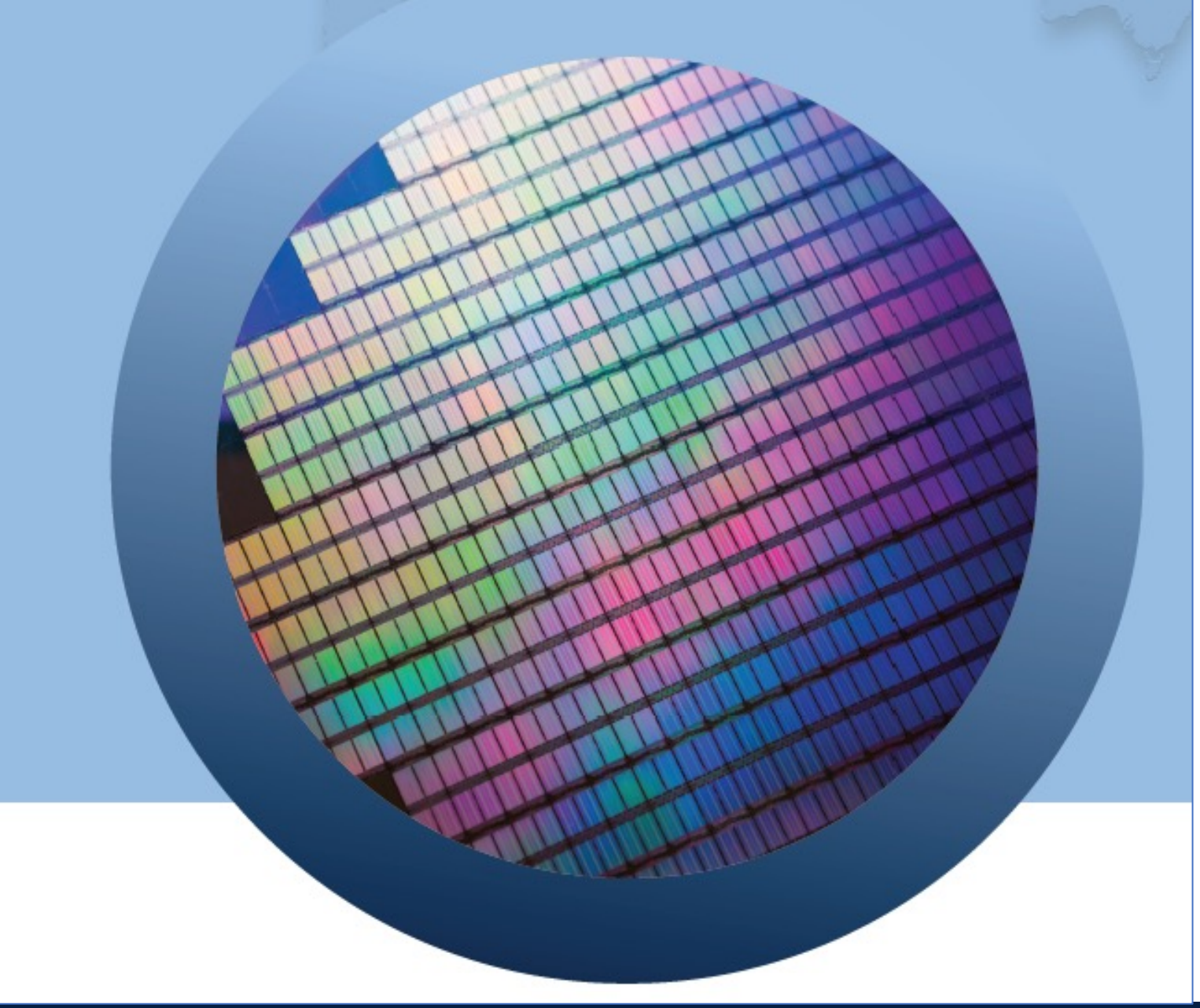


CHIPS @ Penn State

Town Hall
1 Mar 2023

Lora G. Weiss, Ph.D.
Senior Vice President for Research

Town Hall Agenda

8:00 - 8:20	Opening statements and update on CHIPS programs	Lora Weiss
8:20 - 8:40	MASH & CHIPS Act: Summary of activity to date & next steps	Daniel Lopez
8:40 - 9:00	Materials, facilities, and industrial needs	Susan Trolier-McKinstry
9:00 - 9:20	How packaging is critical to the CHIPS Act program	Madhavan Swaminathan
9:20 – 10:00	Open Discussions	

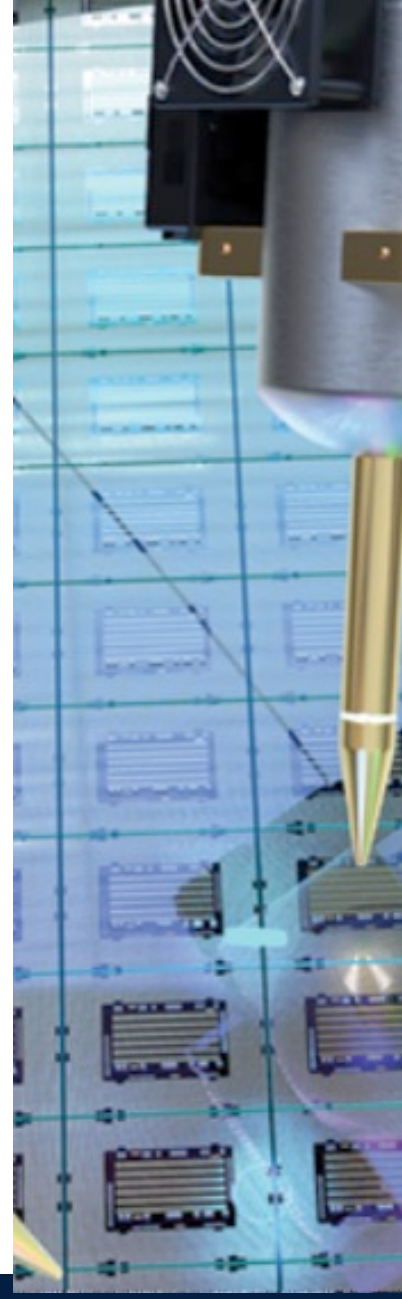
CHIPS Organizing Team

Phil Savage, Lead

Daniel Lopez

Madhavan Swaminathan

Susan Trolier-McKinstry



CHIPS + Science Act of 2022

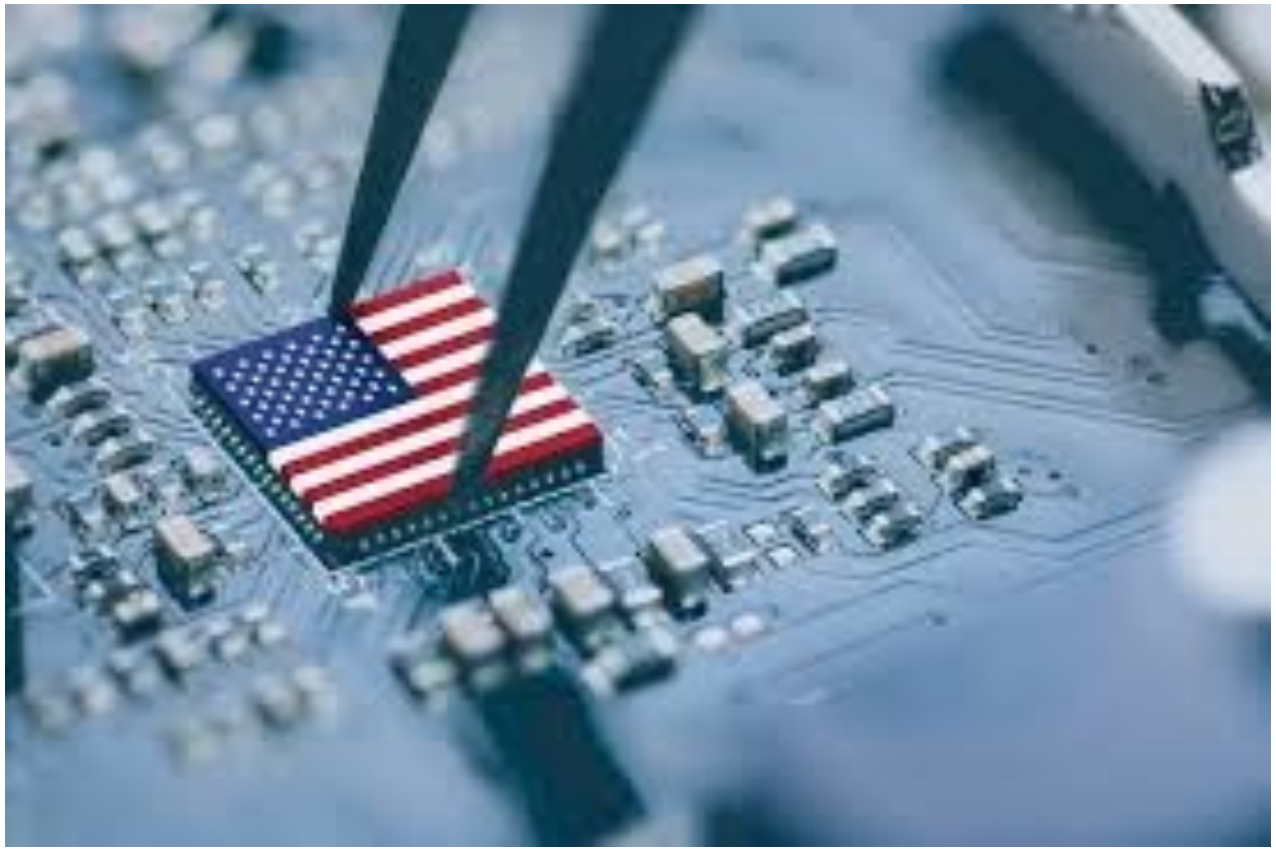


Photo credit: https://www.brookings.edu/research/the-potential-of-the-chips-and-science-act-for-rural-america/

THE WHITE HOUSE

AUGUST 25, 2022

Executive Order on the Implementation of the CHIPS Act of 2022

"The CHIPS and Science Act will boost American semiconductor research, development, and production, ensuring U.S. leadership in the technology that forms the foundation of everything from automobiles to household appliances to defense systems."

Source: https://www.whitehouse.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china/

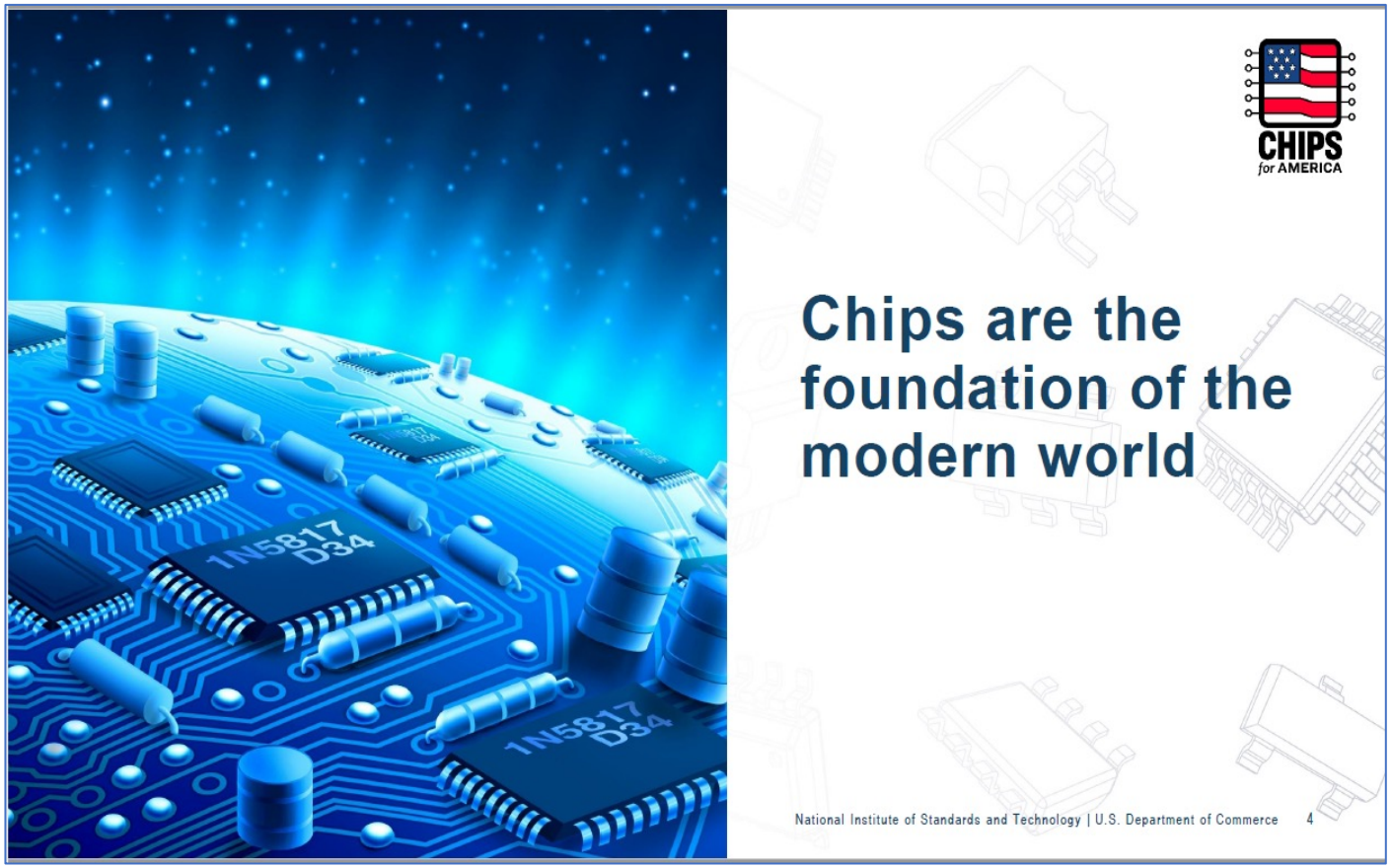
What Is in It?

Source: https://www.mckinsey.com/industries/public-and-social-sector/our-insights/the-chips-and-science-act-heres-whats-in-it

- Directs $280 billion in spending over the next ten years
  - $200 billion for scientific R&D and commercialization
    - STEM
    - R&D
    - Workforce Development
    - Economic Development
  - $24 billion in tax credits for chip production
  - $3 billion for supply chains
  - **$50+ billion for semiconductor manufacturing, R&D, and workforce development**
  - and more

- Authorizations at
  - National Science Foundation
  - Dept of Energy
  - Dept of Defense
  - Dept Commerce

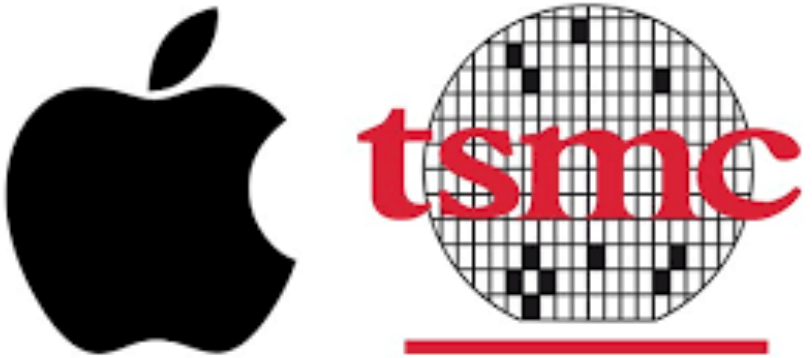
Setting the Stage: 30,000 Feet



- We are at a unique time in history for R&D
  - 1st time in many of our careers where the government has made a dedicated, concerted, focused effort to invest in and advance a research area of such critical importance and ***at the scale that is planned*** for semiconductors
- Semiconductors continue to define the world we live in
  - From geopolitics to the global economy and across the spectrum of military power
- Three Pillars
  - Economic Security
  - National Security
  - Future Innovation

30,000 Feet – cont'd

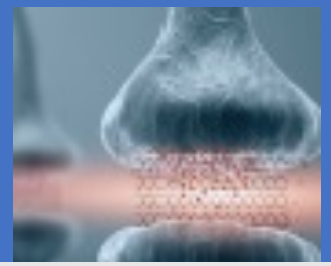
- Nearly 1/4 of the chip industry's revenues come from smartphones
- Smartphones have more than a dozen chips in them, controlling multiple sensors
  - Bluetooth, WiFi, cameras, accelerometers, and more
- Apple designs their chips; it does not make any of them
- The most advanced chips that Apple uses are made in one place in the world, at TSMC in Taiwan
- Apple's A-series microprocessors have nearly 12 billion transistors.
  - In 1961, chips had only 4 transistors
- Although R&D is done in the US, we continue to outsource ***assembly, testing, and packaging (ATP)***



CHIPS R&D Challenges

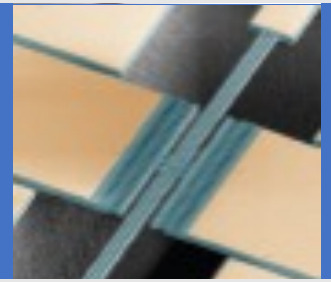
- Fabricating and miniaturization is an engineering challenge
- Advances in Electronic Design Automation are needed
  - Use software to design how millions of transistors are laid out on a chip and then simulate their operation
- Low cost, highly reliable packaging
  - Critical to putting thousands of chips into daily use
- Need new materials, thin films, and photonics
- Need synthesis of materials for power electronics, integration of ferroelectrics with semiconductors, and glass packaging for quantum sensing
- We are uniquely positioned to do research on 8” wafers
- And we will accelerate transition of chip advances into the manufacturing process
- + much more

Penn State Strengths in Materials Research



2D Semiconductors

Ferroelectric Microelectronics

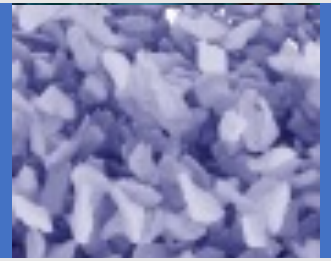


Micro Electro-Mechanical Systems

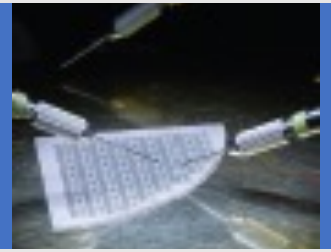
Organic Semiconductors

Internet of Things

Quantum Packaging



Packaging Solutions



Wide Band Gap Semiconductors

CHIPS Workforce Challenges (from Secretary Raimondo's Comments)

- Increase pipeline of skilled workers to power the US Chip ecosystem
  - From technicians to PhDs
  - Those without college degrees get high paying jobs
- Create high paying jobs across the country, not just cities
- Inspire a generation of engineers and scientists to go into manufacturing
  - Colleges should triple number of graduates in semiconductor fields including engineering
  - Want them to be ready to work on day 1
- Align programs with fabs, with student internships for hands on experience
- Train 100,000 people in the next decade
- Open pipeline to women, veterans, people of color

https://www.psu.edu/news/impact/story/penn-state-offers-free-live-stream-nanotechnology-workshops/

Industry Collaborations - Critical

- In 1958, Jack Kilby co-invented the integrated circuit
  - In 2000, he won the Nobel prize for it
- He was at Texas Instruments, doing research
  - Began collaborating with universities and companies
- Early example of the importance of Industry-University-Government collaborations
- Need to work closely with fabs
  - Any R&D advances must transition
- Recognize high cost of changing tools and processors
  - This is where our industry and government partnerships will be key

https://www.pbs.org/video/the-chip-that-jack-built-t401cq/

Funding Opportunities…What We Know So Far

Agency	Program(s)		FY22	FY23	FY24	FY25	FY26	FY27	Total
Commerce	Manufacturing Incentives		$19 B	$5 B	$5 B	$5 B	$5 B	-	$39 B
Commerce	R&D	NSTC NAPMP Manu USA Inst NIST Metrology	$2 B $2.5 B $500 M	$2 B	$1.3 B	$1.1 B	$1.6 B	-	$11 B
Defense	Microelectronics Commons		-	$400 M	$400 M	$400 M	$400 M	$400 M	$2 B
NSF	Workforce and Education Fund		-	$25 M	$25 M	$50 M	$50 M	$50 M	$200 M

Single Wick vs. Microchip…Who's Fresher?

Thank You

Febreze Fade Defy Plug | Single Wick vs Microchip... Who's Fresher?

MASH & CHIPS Act
Summary of activity to date & next steps

Daniel Lopez
Materials Research Institute
Electrical Engineering

CHIPS and Science Act (Department of Commerce)

$11 billion for R&D

- National Semiconductor Technology Center
- National Advanced Packaging Manufacturing Program
- Manufacturing USA Semiconductor Institute(s)
- National Institute of Standards and Technology measurement science

A domestic infrastructure for research, prototyping innovations and packaging

R&D collaborations between academia and industry

Workforce development and training/education

Facilities and equipment

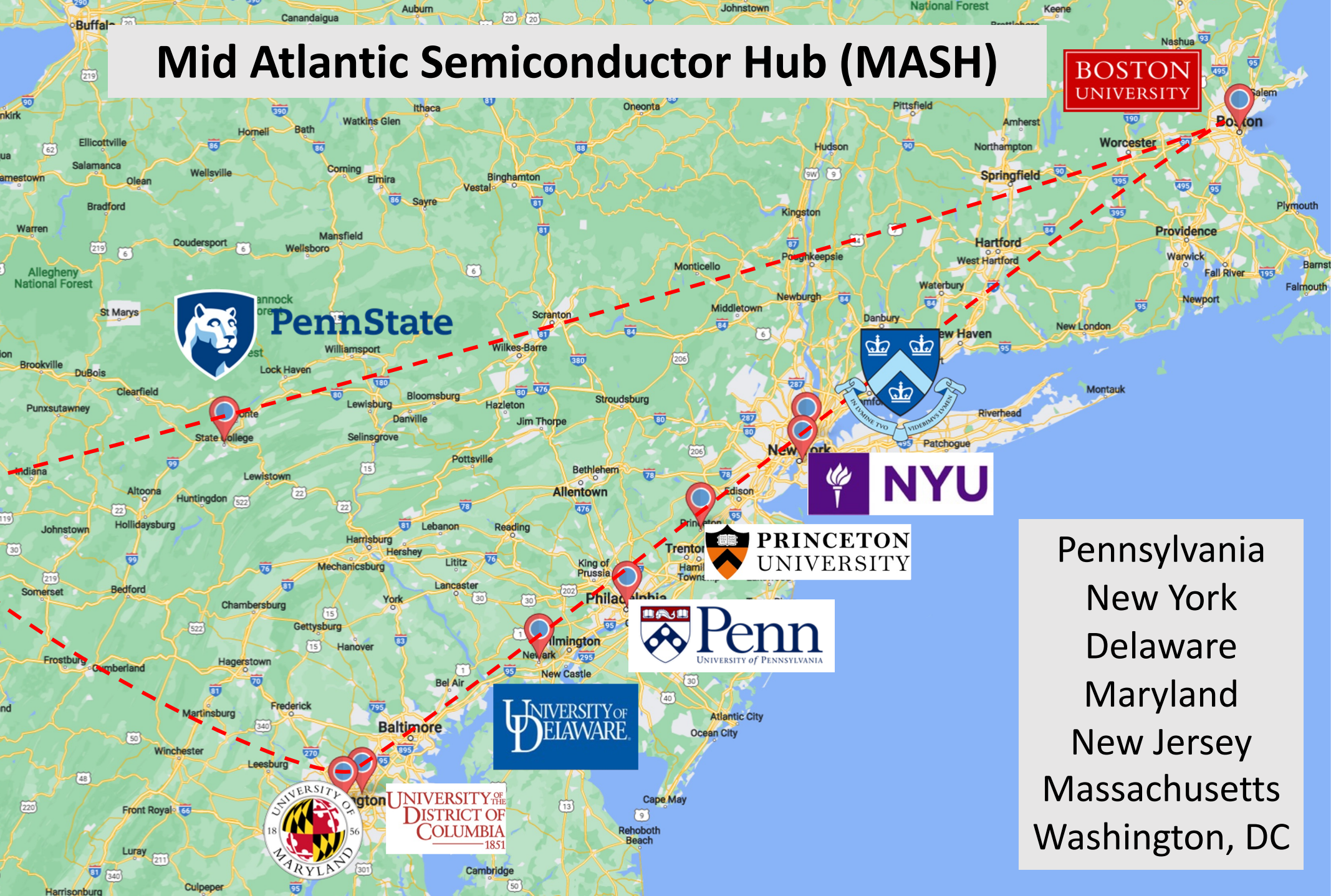
Advanced packaging and testing

Metrology and characterization

Advanced manufacturing

Workforce development

Mid Atlantic Semiconductor Hub (MASH)



Mid Atlantic Semiconductor Hub (MASH)

MASH Purpose

Create a **collaborative coalition** of top universities and industries that can **combine resources and expertise** to meet the need of semiconductor industry in the US by strengthening and aligning research, manufacturing, and workforce development.

MASH Mission and Vision

MASH will enable a vital and growing silicon and silicon-adjacent industry base in our region and beyond to work with universities to:

- increase domestic semiconductor manufacturing across all sectors;
- translate cutting-edge research into industry manufacture; and
- educate the future semiconductor workforce across all levels (universities, 4 & 2 year colleges, and pre-college internship programs)

We will achieve this by creating a network of smart and agile industry/university pre-manufacturing infrastructure nodes to accelerate CHIPS innovation and deliver workforce development across the supply chain for semiconductors, packaging, and components.

The mid-Atlantic is not currently slated for a large silicon chip fabrication facility.

However, there are many other manufacturing pieces that enter into silicon-enabled products - and our region is rich with these technologies

- Materials and materials integration
- Semiconductor equipment manufacture
- Prototyping equipment
- Power components and module power delivery
- III-V devices
- Packaging
- …

Silicon Adjacent Technologies

MASH kick-off workshop: January 11, 2023 @ UPenn

Collect **industrial** feedback on

How our combined research, educational activities, and resources would be helpful to support and enhance the future of US semiconductor research and manufacturing?

- Most of the speakers from the industry
- 106 attendees from industry (57 companies)
- 149 academia
- 12 government officials
- 20 institutions

Challenges to build a new semiconductor ecosystem

A domestic infrastructure for research, prototyping & packaging

Challenges

- US university infrastructure outdated
  - Limited capability to support US government and industry needs
- It takes more than 5 years to design, build and operate a new state-of-the-art facility
  - universities must leverage on existing fabrication, metrology and packaging facilities
- US needs some "*optimal*" university facilities for fab, prototyping and packaging

R&D collaborations between academia and industry

Challenges

- Silicon-adjacent technologies
- Improve the alignment between industry needs & higher education outcomes
- Develop metrology for next generation of semiconductor materials and devices
- Identify industrial challenges that require fundamental and applied research
- Develop novel approaches to simplify IP generation and knowledge sharing

Workforce development and training

Challenges

- Develop a modern semiconductor curriculum in partnership with industry and across regional hubs
- Modernize education infrastructure
- Facilitate quick access to specialized training and WFD
- Diversity, equity and inclusion: train a broad diversity of students, technicians and apprentices
- Talent retention: low salaries and poor work/life balance

DoC – NIST: Request for Information
Manufacturing USA Semiconductor Institutes

FEDERAL REGISTER
The Daily Journal of the United States Government

Notice

Manufacturing USA Semiconductor Institutes

A Notice by the National Institute of Standards and Technology on 10/13/2022

Under Section 9906(f) of the CHIPS for America Act, the Director of NIST may establish up to three Manufacturing USA Institutes described in section 34(d) of the NIST Act (15 U.S.C. 278s(d)) that are focused on semiconductor manufacturing. In addition, the Secretary of Commerce may award financial assistance to any Manufacturing USA institute for work relating to semiconductor manufacturing. Such institutes may emphasize the following:

(1) Research to support the virtualization and automation of maintenance of semiconductor machinery.

(2) Development of new advanced test, assembly and packaging capabilities.

(3) Developing and deploying educational and skills training curricula needed to support the industry sector and ensure the United States can build and maintain a trusted and predictable talent pipeline.

Manufacturing USA Semiconductor Institutes

This document is responsive to the Department of Commerce - NIST Request for Information (RFI) on *Manufacturing USA Semiconductor Institutes* (released 10/13/22) and is the result of collaborative efforts among the following universities:

- Penn State University (PA)
- University of Pennsylvania (PA)
- Carnegie Mellon University (PA)
- Columbia University (NY)
- New York University (NY)
- University of Maryland (MA)
- Princeton University (NJ)
- University of Delaware (DE)
- Boston University (MA)
- University of the District of Columbia (DC)

In addition, we have multiple inputs from collaborators and partners across a broad ecosystem of industries, all levels of education and workforce training, National Labs, and government and economic development organizations.

I. Institutes Scope

Role of the Manufacturing USA Semiconductor Institutes

The Manufacturing USA Semiconductor Institutes should lead, coordinate, and provide access to advanced educational and R&D infrastructure to a network of organizations dedicated to accelerating and improving the pace of semiconductor innovation and translation. The Semiconductor Institutes (SI) will have a unique role in the constellation of Manufacturing USA Institutes due in part to the well-identified needs associated with workforce development in the semiconductor industry. Although in principle, all Institutes have some associated component of workforce development, the SI will need to address a much deeper deficit in qualified workers across the entire educational spectrum when compared with many other industries. To this end, an Institute structure involving tighter cooperation between industry and academia is appropriate, such as industry-informed curriculum development and development of alternative certification pathways at all academic institutions: research universities, 4-year and 2-year colleges, and technical training (and re-training) programs. In addition, due to the cutting-edge and continually-evolving nature of the semiconductor industry, the SI should lead, coordinate, and provide access to advanced R&D infrastructure to a network of organizations – industry, national laboratories, and academia - dedicated to accelerating and improving the pace of semiconductor innovation and translation.

We note that the National Science Foundation has a highly successful program honed over decades that fosters university and industry engagement toward, and workforce development for, a common applied goal. This program, the Engineering Research Center (ERC), is based on academia-led engagement with industry, and typically focuses much of its workforce development on undergraduate and graduate education. The structure of the SI could be informed by this ERC

RFI for Manufacturing USA Semiconductor Institute(s)
https://www.regulations.gov/document/NIST-2022-0002-0001

12 December 2022: 94 submissions

MANUFACTURING USA SEMICONDUCTOR INSTITUTE FOCUSED ON ADVANCED PACKAGING FOR ADVANCED COMMUNICATIONS RESPONSE TO REQUEST FOR INFORMATION (RFI)

Authored by: Madhavan Swaminathan (Georgia Tech/Penn State), Andrew Ketterson (Qorvo), Jeb Flemming (3DGS), Babu Mandava (3DGS), Lee Smith (Applied Materials), Martin Letz (Schott), Aric Shorey (Menlo Microsystems), Ravikumar Katare (Corning), Jun-Ro Yoon (Corning), Ming Zhang (Synopsys), Urmi Ray (iNEMI), Osama Awadelkarim (Penn State), Daniel Lopez (Penn State), Tim Lee (Boeing), Sungjin Kim (Absolics), Aiden Oh (Absolics), Volker Sorger (GWU), Jesse Bonfeld (Schott)

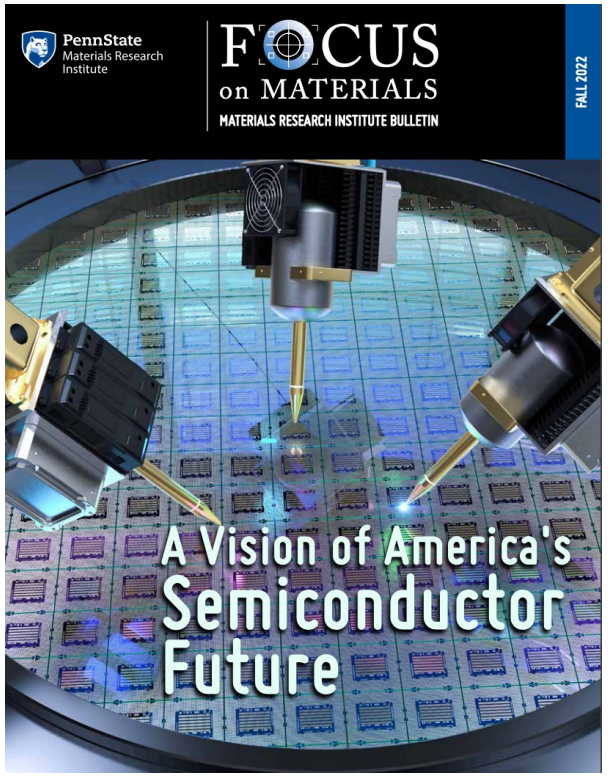
The global semiconductor industry is projected to become a trillion-dollar industry by 2030 driven primarily by computing, data storage, wireless, and automotive applications [1]. This is historic considering that it took the industry 55 years to reach half a trillion dollars in size and will take just another 10 years or less to double in size to a trillion dollars. Since semiconductors will power the next decade of global growth in an increasingly data-hungry world, much like oil fueled the rise of industrial economies in the last century [2], the US needs to position itself and continue to be a global leader not just in design but also in manufacturing. This response to RFI is a positioning statement for establishing a Manufacturing USA Semiconductor Institute by bringing together academia, national laboratories, industry, and government that can help fuel innovation and establish US leadership.

The 2018 Basic Research Needs for Microelectronics report by the office of science articulates the need for flipping the current paradigm whereby innovative materials, devices, and architecture requirements are driven by applications, algorithms, and software [3]. The *2021 NSF Workshop on Future of Semiconductors and Beyond: Devices & Technologies* argues that there is a need for a system driven effort that can fuel technology development and the end-product in university research should drive US competitiveness in manufacturing [4]. The *2021 AI-Enhanced Co-Design for Next-Generation Microelectronics: Innovating Innovation Workshop* organized by Sandia National Laboratory amplifies the need for a co-design approach to identify opportunities for transformative advances in microelectronics [5]. Based on the need for applications driving discovery, inter-disciplinary research enabling innovation and manufacturing being the end-product, we propose the establishment of a manufacturing USA institute, that enables a semiconductor eco-system to further US competitiveness, that specifically targets **advanced packaging and substrate technologies**. We further propose that **communications and sensing** are key drivers for the growth of the semiconductor industry with relevance to both commercial and defense sectors. We see applications in advanced communications as a key driver of new technologies in packaging that requires innovative heterogeneous integration solutions to bring together disparate process nodes and technologies. With 6G already on the horizon and new applications emerging in radar imaging, sensing, virtual reality, artificial intelligence, pervasive connectivity, and others, the need for higher data rate will only increase requiring larger bandwidth systems operating at higher frequencies. **We therefore target sub-Terahertz (beyond 100GHz) wireless applications as the primary driver for defining new packaging technologies, that can ultimately find their way into manufacturing.**

We provide responses under the five broad categories posed by NIST and try to answer as many of the 28 questions raised (marked **Q1 to Q28** in this document).

I. INSTITUTE SCOPE

Marketing and public involvement



Jennifer McCann
Materials Research Institute

Jamie Oberdick
Materials Research Institute

Bob Cornwall
Materials Research Institute

Workforce Development

MASH Mid-Atlantic SEMICONDUCTORS HUB

A key to America's future semiconductor success story will be building a skilled workforce, a well-prepared set of workers to address the needs of the chips industry. Workforce development is an essential part of the Chips and Science Act, designed to meet the needs of the semiconductor industry.

Overall, educational institutes and universities can play a crucial role in preparing students for careers in the semiconductor sector by providing them with a strong foundation in STEM skills, hands-on experience, industry connections, and professional development opportunities.

- Many of our university partners offer **courses and programs** that focus on the science, technology, engineering, and mathematics (STEM) skills needed for the semiconductor industry.
- The MASH hub partners offer labs, **co-op programs**, **internships**, and other opportunities for students to gain **hands-on experience** working with semiconductor technology. This can help students **develop the technical skills and knowledge** needed for a career in the industry.
- Industry and universities partner together in semiconductor technologies which can help to provide students with exposure to the latest technologies and industry trends. These partnerships can also provide students with **networking opportunities** and **potential job prospects**.
- There is access to **state-of-the-art research opportunities** where students can work on projects related to semiconductor technology and gain an in-depth understanding of the field.
- As part of workforce development in the MASH hub, we offer **professional development opportunities** such as workshops, seminars, and other training to help students develop the soft skills, such as communication, teamwork, and problem solving, that are needed to succeed in the industry.

Highlighted workforce development programs

Penn State
Teaching the next generation at the Center for Nanotechnology Education and Utilization
The 2-Dimensional Crystal Consortium Resident Scholar Visitor Program: 2DCC RSVP
The Research Experience for Undergraduates Program: Scalable Nanomanufacturing of Complex Materials
Retraining the military personnel

Other University Partners

February 2022

Lora Weiss suggestion

About the HUB

MASH Mid-Atlantic SEMICONDUCTORS HUB

Research

MASH Mid-Atlantic SEMICONDUCTORS HUB

MASH Areas of Research for America's Semiconductor Future

Digital Twinning

In the context of semiconductor manufacturing, digital twinning can be used to improve the efficiency, quality, and yield of th process, identify bottlenecks and inefficiencies, and test different scenarios to optimize the process. This can help to reduce t final product.

Recent research in digital twinning:
Digital Innovation Lab – the lab will help local industry partners develop digital "twinning," the simulated representation of a p
SMORES-EP – Designing autonomous robots that change shape to adapt to challenging environments

Quantum Packaging

We have multiple research activities focused on designing dielectric materials for high frequency and high thermal conductivi that can be assembled with multilayer structures and or 3D printed structures packaging devices. Combining new processing significantly overcome limitations with traditional packaging solutions.

PennState

PSU Strengths: Materials, Facilities, and Coupling to Industry Needs

Susan Trolier-McKinstry

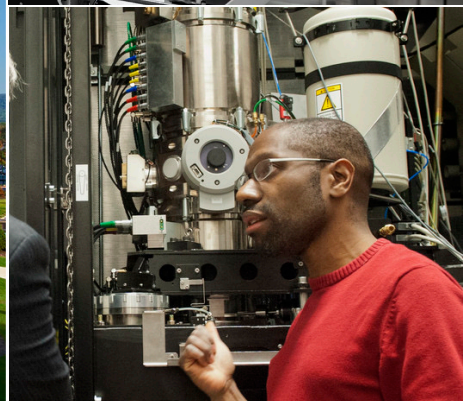
PennState

Starting Assumptions and a Caveat

- We are more likely to get significant funding if we can show areas of strength, where Penn State and its partners are the obvious place for investment.
  - I have not covered excellent single investigator efforts here
- The CHIPS act is intended to increase US commercial competitiveness
  - Groups that can point to an industry-pull may be more likely to be funded than those that point only to basic research
- I had 4 days to put this together, and where I have missed areas of strength, it is in ignorance, not malice. PLEASE respond to the RFI that will be coming out, so that your efforts can be included!

PSU Strengths: Integrated Infrastructure

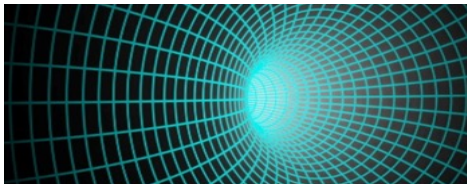
- Highly interdisciplinary research milieu
- #1, #2 in expenditures in Materials Science and Materials Engineering
- ARL facilities offer significant scaling options
- Strong programs in workforce development exist in the College of Education, Penn College, CNEU, ARL, etc.



Labs co-located in state-of-the-art building on central campus

Four Lab Solution: Theory, Synthesis, Fabrication, Characterization

MCC



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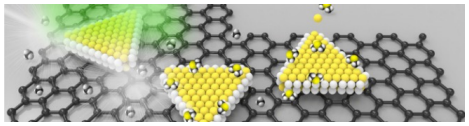
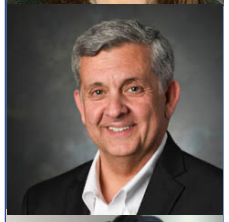
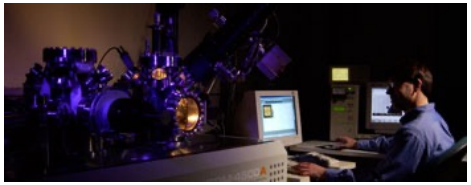




Nanofab

Materials Characterization Lab

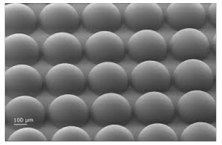


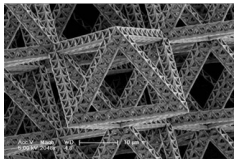
Evaluate material candidates

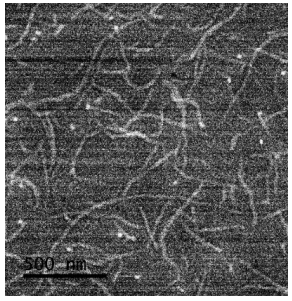
Synthesize materials

Fabricate Devices/ Structures

Characterize materials







PennState

Facilities, Education and Outreach

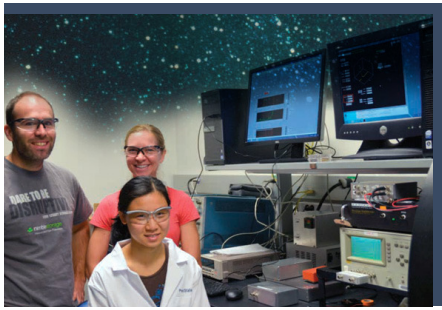
Goals

1. Prepare a talented and diverse workforce
2. Enable outstanding research and education
3. Enhance public awareness of science and technology

Activities

1. Multiple courses run in the facilities, including Materials Characterization, and Semiconductor Integrated Circuit Technology
2. Graduate Student and undergraduate research relies on technical staff for training, safety, and tool maintenance
3. **Many tools allow remote access for remote workforce development**
4. Webinar series and workshops

Graphene and Beyond Workshop

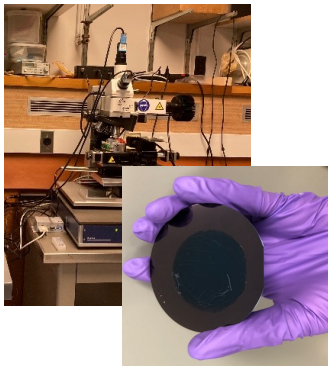



PennState

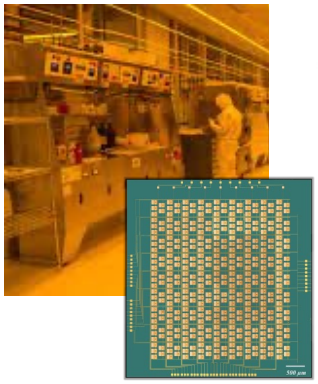
2D Crystal Foundry (2DCF)

Translational research and workforce training for emergent 2D material platforms

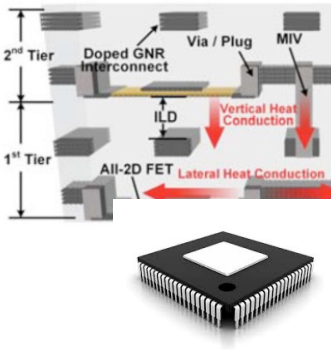
Crystal growth & epitaxy



2D layer transfer & stacking



Device and circuit fabrication



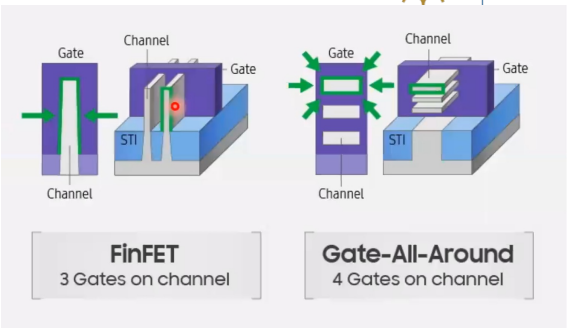
Heterogeneous integration & packaging

AI-assisted process control and comprehensive data infrastructure

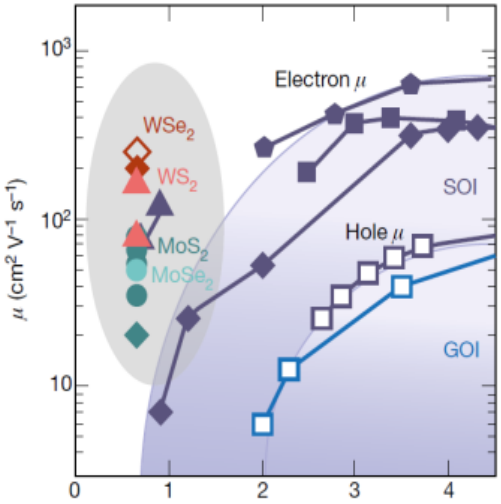
2D CMOS enables Moore's Law Scaling and CMOS + X

2D FETs are part of semiconductor roadmap for scaling of stacked **nanosheet** devices.

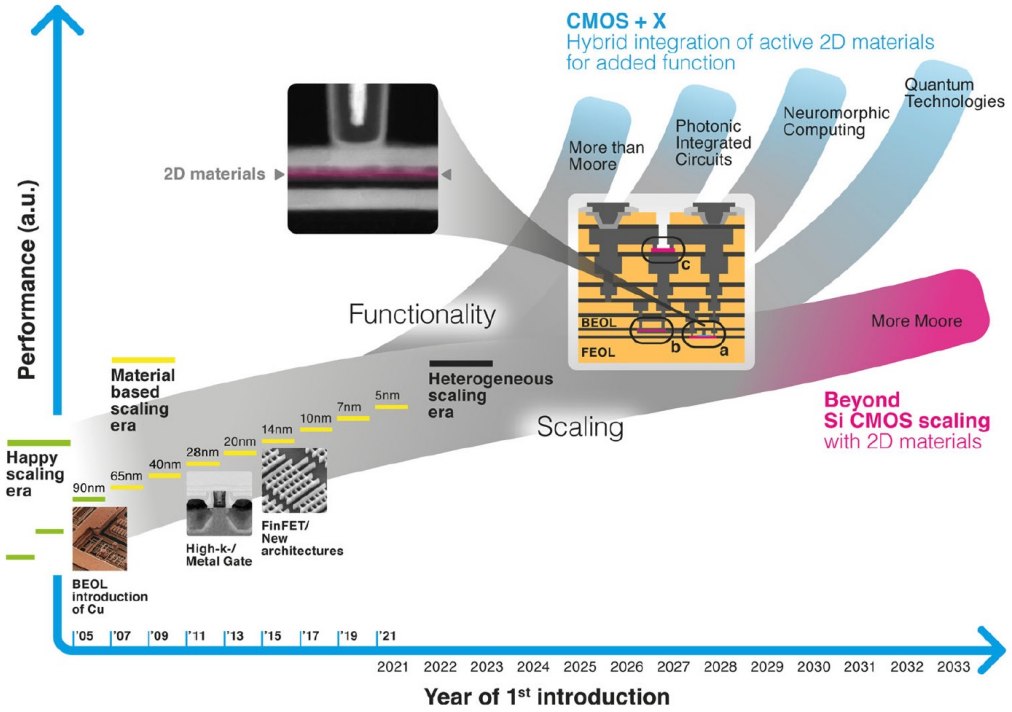
2D CMOS offers enhanced gate pitch scaling – Can stack a greater number of 2D sheets in given area than comparable Si devices



Higher mobility in 2D compared to si for ultra-thin nanosheet channels



D. Akinwande, et al. Nature 573 (2019) 507.

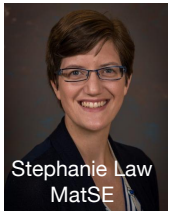


Why Penn State in 2D Materials?

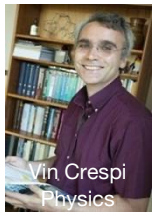
- PSU clear **worldwide leader in 2D** beyond graphene
- Interdisciplinary faculty involvement (**25+ faculty, > 100 students/postdocs**)

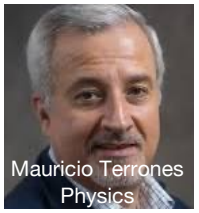

Joan Redwing MatSE


Josh Robinson MatSE


Stephanie Law MatSE


Nitin Samarth Physics


Vin Crespi Physics


Mauricio Terrones Physics

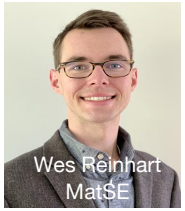

Zhiqiang Mao Physics

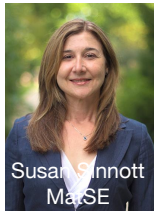

Jun Zhu Physics

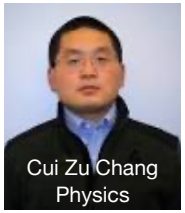

Suzanne Mohnney MatSE

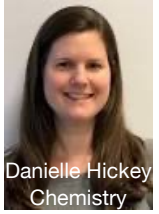

Nasim Alem MatSE

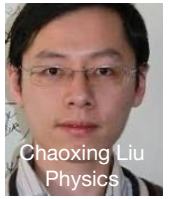

Venkat Gopalan MatSE


Wes Reinhart MatSE


Susan Sinnott MatSE


Cui Zu Chang Physics


Danielle Hickey Chemistry

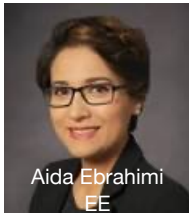

Chaoxing Liu Physics


Ying Liu Physics

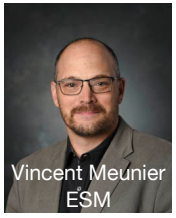

Saptarshi Das ESM


Adri van Duin Mech Eng


Slava Rotkin ESM


Aida Ebrahimi EE


Doug Wolfe ARL/MatSE

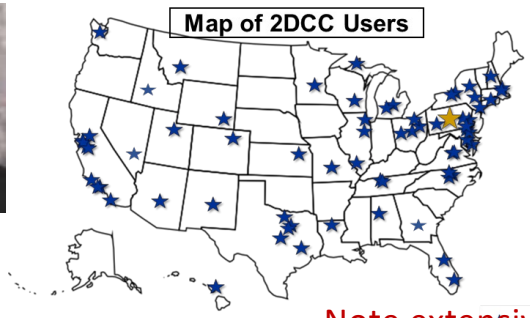

Vincent Meunier ESM


Morteza Kayyalha EE


Yang Yang ESM


Tom Jackson EE


Yuan Xuan MechEng



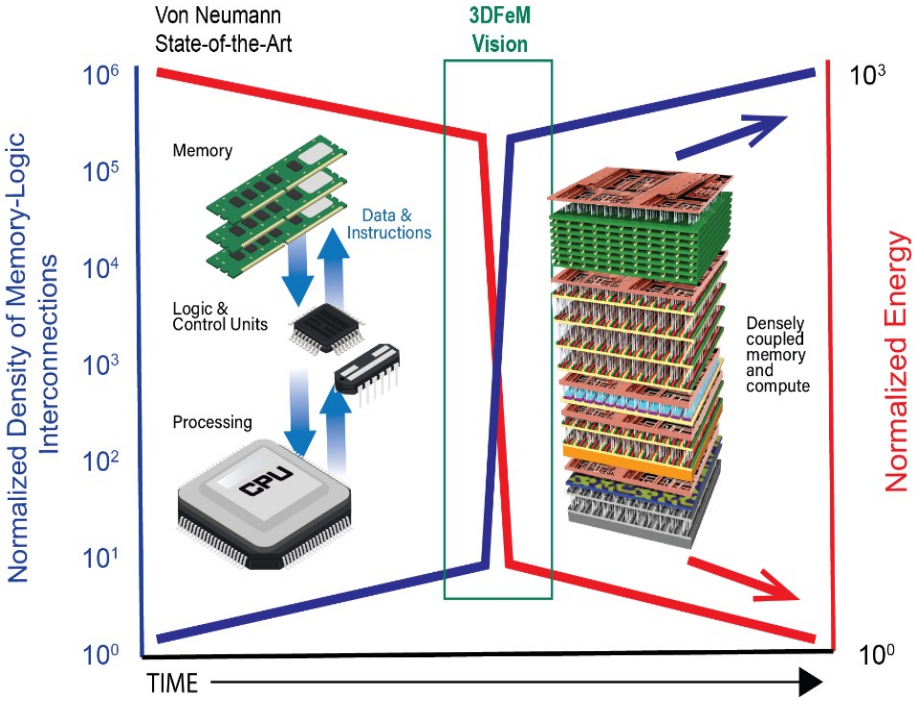
Note extensive network in mid-Atlantic region
(PSU, UPenn, Columbia, CMU, etc.)

Industry collaborators: Intel, TSMC, Aixtron

Silicon Adjacent Technologies: Integrating Ferroelectrics with Semiconductors

With faculty from MASH partners

- Computing accounts for 5 – 15% of worldwide energy consumption
- US data centers consumed ~73 billion kWh in 2020
- This is being exacerbated by needs for big data for machine learning, personalized health, data analytics, fast back-up and restore
- Integrated, close-couple ferroelectric non-volatile memory offers a solution



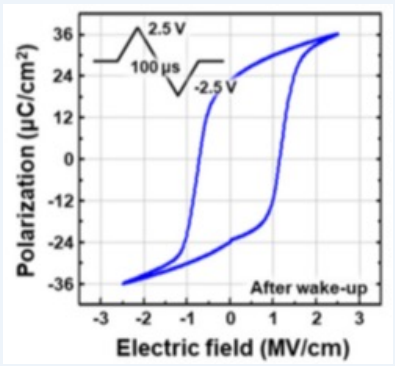
3D FeM

U.S. DEPARTMENT OF ENERGY | Office of Science

New Ferroelectrics for Non-volatile Memory

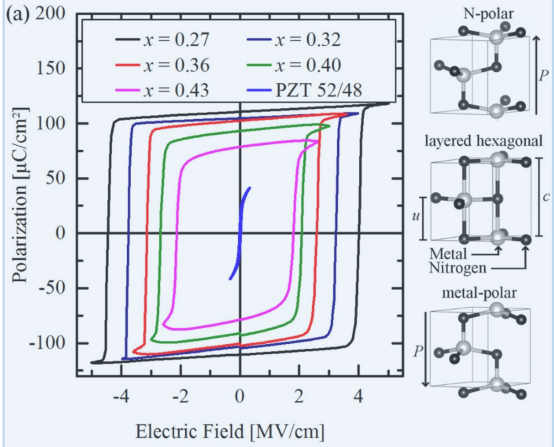
Common link: Electromechanical property **boost** at verge of composition **instability**

$Hf_{1-x}Zr_xO_2$



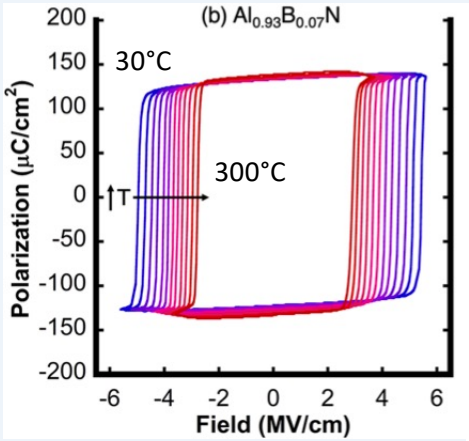
Muller et al., IEDM Proc., and APL (2011)

$Al_{1-x}Sc_xN$



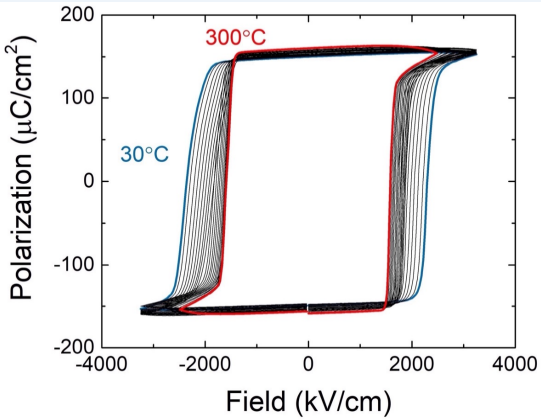
Fichtner et al., J. Appl. Phys. 125, 114103 (2019)

$Al_{1-x}B_xN$



Hayden et al., Phys. Rev. Mat. (2021)

$Zn_{1-x}Mg_xO$



Ferri et al., JAP (2021)

This team has key expertise in the deposition, patterning, characterization and modeling of these materials!

3D FeM

U.S. DEPARTMENT OF ENERGY | Office of Science

Piezoelectrics Microelectromechanical Systems

Sensors

- High e_{ijk}/ε_r for voltage-based sensors
- High e_{ijk} for charge-based measurements
- High signal to noise ratio

$$\frac{e_{ijk}}{\sqrt{\varepsilon_o \varepsilon_{ij} \tan\delta}}$$

Actuators

- High e_{ijk}
- High drive field capability
- Stability

Piezoelectronic Transistors

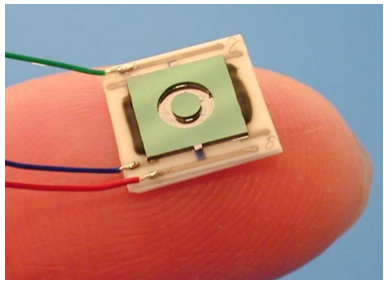
- High d_{33}
- High saturation strains

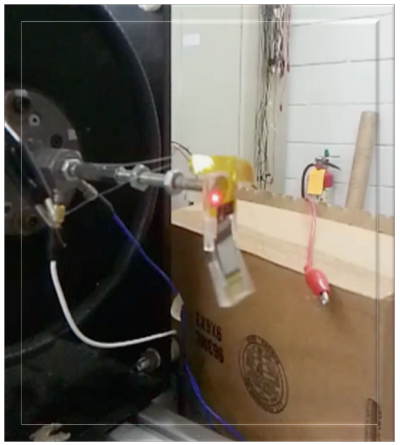
Energy Harvesting

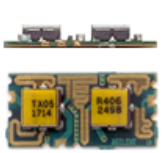
- High $k^2 \propto e_{ijk} h_{ijk}$
- Low mechanical losses

Resonators

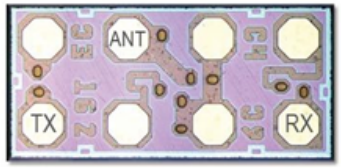
- High k^2Q
- Temperature Stability





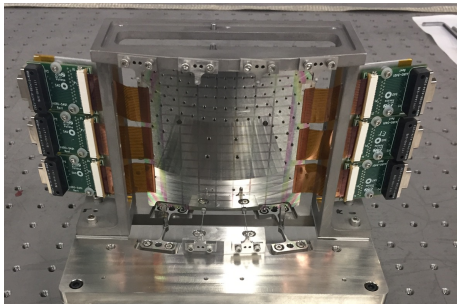


Size relative to first Gen. FBAR Duplexer

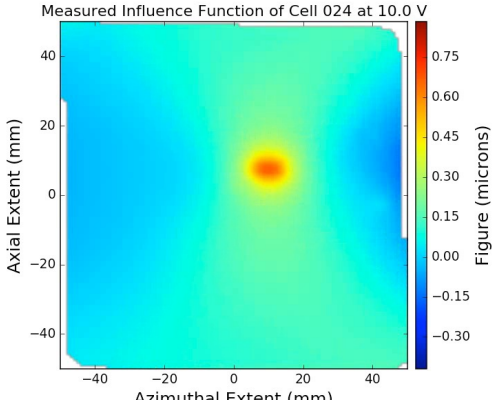


FBAR 1st Gen. Solution:
2 mm high
6 x 12 mm footprint

FBAR 3rd Gen. Solution:
0.23 mm high
0.7 x 1.5 mm footprint



IF Calibration for AXRO Test Piece



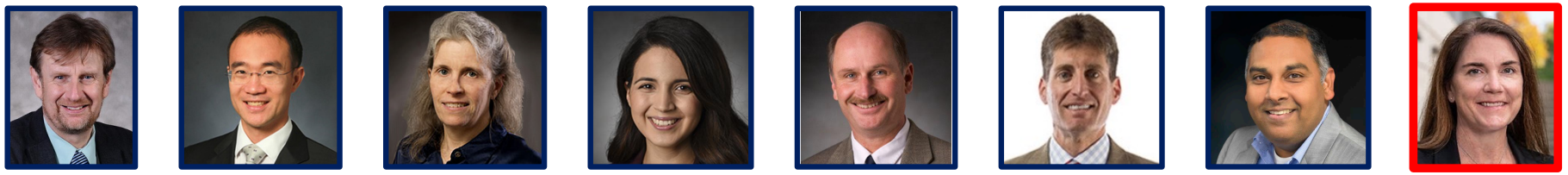
Electronics + MEMS is transformational

Piezoelectrics and Piezoelectric MEMS

Partnered with many companies

- Penn State has been the world-leading institution in piezoelectrics for decades
- US is lagging significantly in investing in piezoMEMS foundries relative to Europe and Asia
- Numerous defense-related companies are unable to source legacy bulk piezoelectrics

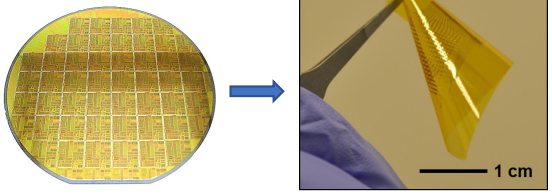
Penn State and Passive Components



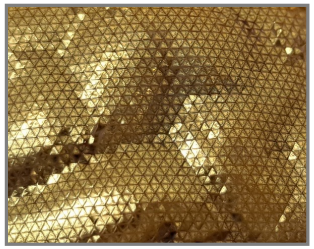
- All circuits require the ancillary passive components! - resistors, capacitors, inductors (1000 capacitors/cell phone, ~15,000 per electronic vehicle)
- Last major US producers of MLCC have been acquired by international entities
- Some Japanese suppliers will not sell parts for US military applications
- Penn State, NC State, University of Sheffield are the core of an NSF IUCRC Center for Dielectrics and Piezoelectrics (CDP) - Carnegie Mellon is affiliated
- 5G/6G materials, new processing, and reliability are key research areas
- Many company partners

More-than-Moore: Flexible Electronics and Heterogenous Integration

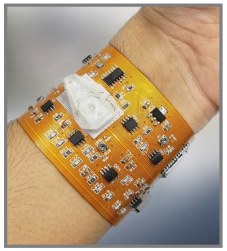
- More-than-Moore device and integration: flexible electronics and hybrid technologies
- PSU has strong expertise and efforts in flexible electronics and heterogenous integration, from multiple semiconductor materials growth, to their heterogenous integration, to device technologies, and to packaging.



Flexible integrated electronics



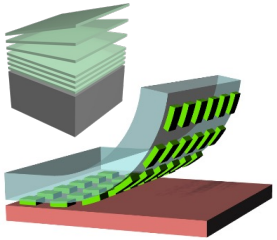
Ultra-thin soft circuits



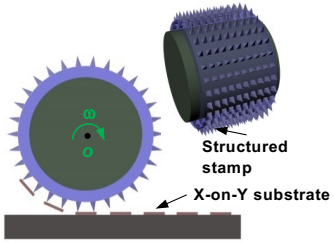
Flexible hybrid electronics

3D Curvy electronics

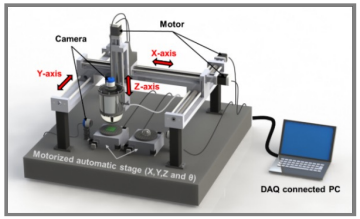
Heterogenous integration



Pick-n-place for semiconductors



Scalable heterogenous integration



CAS printing

PennState

Area of Strength – High Power Electronics including GaN and SiC

The SiC Opportunity & Industrial Impact

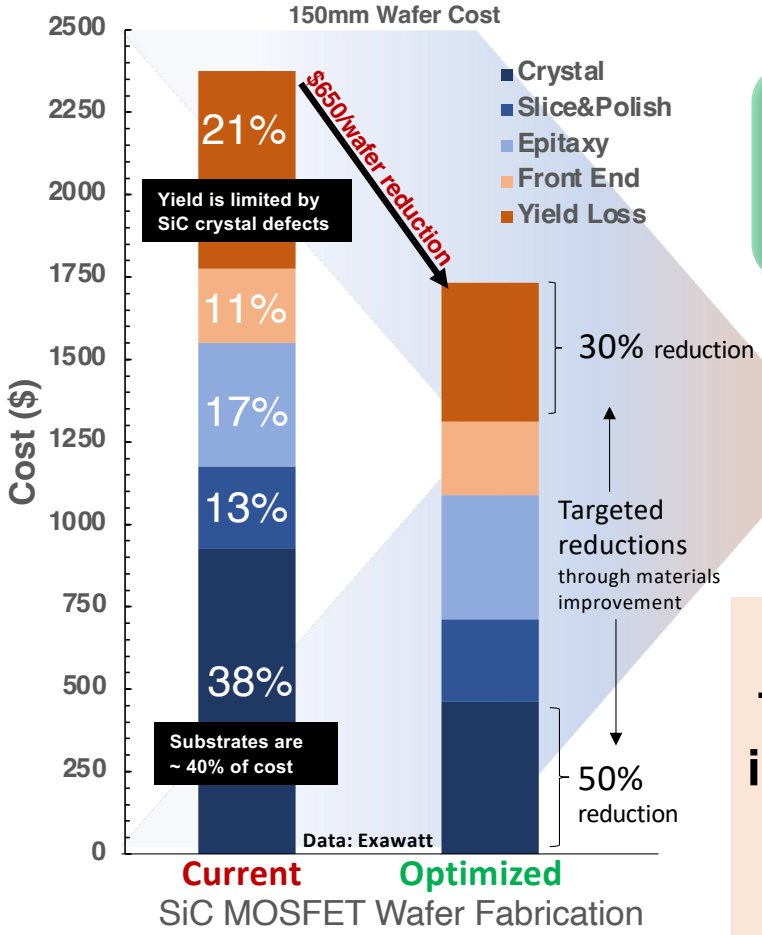
Demand for **SiC** will be >$10B annually by 2030.


Renewable Energy


Electric Vehicles


Data Servers

High Speed Communications



Better crystals lower cost and improve performance.

$1B/year

reduction in mfg. cost

*estimated as $645/wafer, 1.7M wafers/yr by 2025
https://www.semiconductor-today.com/news_items/2021/dec/trendforce-011221.shtml

No platform exists to train the next generation in SiC crystal science and metrology. Penn State intends to be the first.

*10% reduction in both, = $260M/yr
*1% reduction = $26M/yr

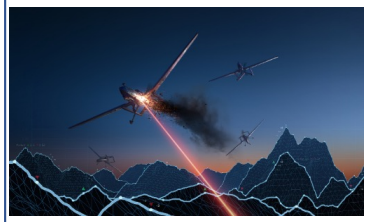
https://www.powerelectronicsnews.com/sic-power-devices-lowering-costs-to-drive-adoption/
https://seekingalpha.com/news/3923289-on-semiconductor-tumbles-william-blair-downgrades-worries-over-yield

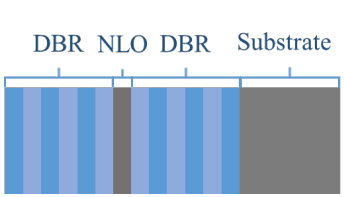
PennState
Applied Research Laboratory

Electronic Warfare

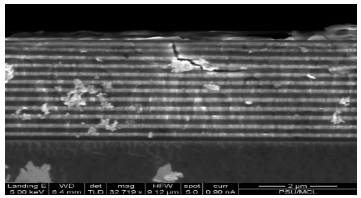
ARL-PSU is currently developing and implementing electronic warfare technologies relevant for DoD CHIPs Efforts

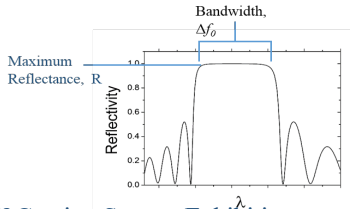
Counter Directed Energy Weapons





Schematic of Counter-DEW Coating System



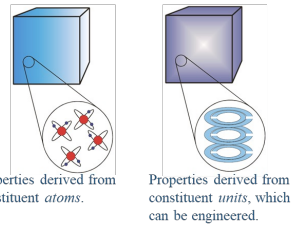


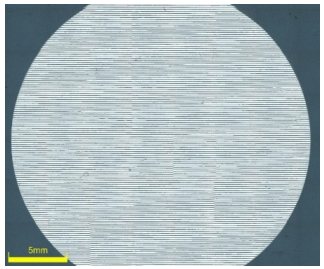
Manufactured Counter-DEW Coating System Exhibiting Broadband Reflectance

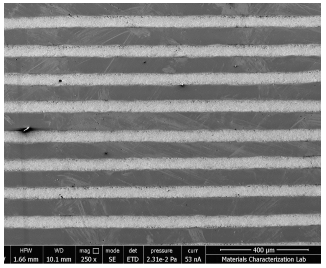
- Multi-layer, highly reflective, reusable coating systems currently being developed for counter-electronic warfare efforts
- Can be incorporated on-chip to protect microelectronic components from electronic warfare interrogation

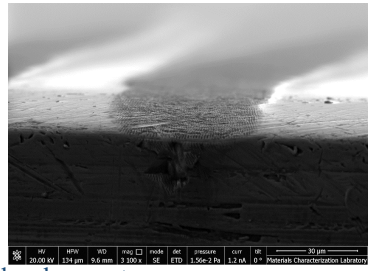
Metamaterials

Conventional vs. Metamaterials









Prototype metamaterial manufacturing development

- Metamaterial-enabled devices have wide ranging applications in RF, THz, IR, and visible spectra
- Can be incorporated into current electronic systems for counter-electronic warfare efforts
- Manufacturing challenges are being investigated at ARL-PSU

High Energy Lasers

High Energy Laser Systems Developed In Collaboration with ARL-PSU

Lockheed Martin

Lockheed Martin

Raytheon Technologies

Radiance Technologies

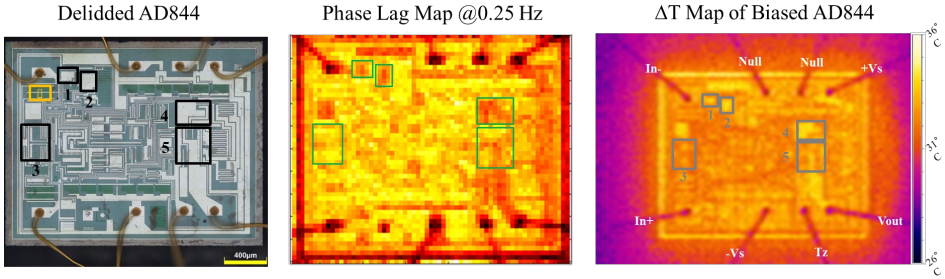
- Identify, test/evaluate, and scale manufacturing processes needed for HEL system deployment
- Bridge technology valley-of-death for new HEL material systems and platforms by leveraging unique manufacturing capabilities housed at ARL-PSU

PennState
Applied Research Laboratory

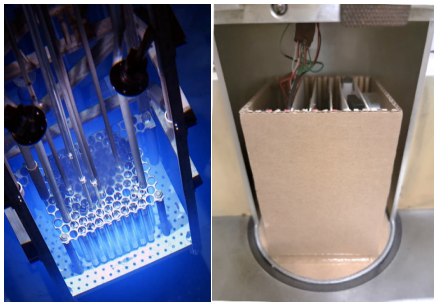
Rapid Characterization of Radiation Hard Electronics

1. ARL-PSU is studying the relative radiation hardness of next generation semiconductors, and developing novel characterization techniques to predict radiation vulnerable regions on chips
2. Ex-situ characterization techniques:
   a) Micro-Raman spectroscopy – strain field mapping
   b) Lock-in Thermography – device level heat/strain mapping
3. In-situ characterization techniques:
   a) Biased γ-ray and neutron testing at application specific doses

Lock-in Thermography of Radiation Sensitive Regions in Electronic Devices

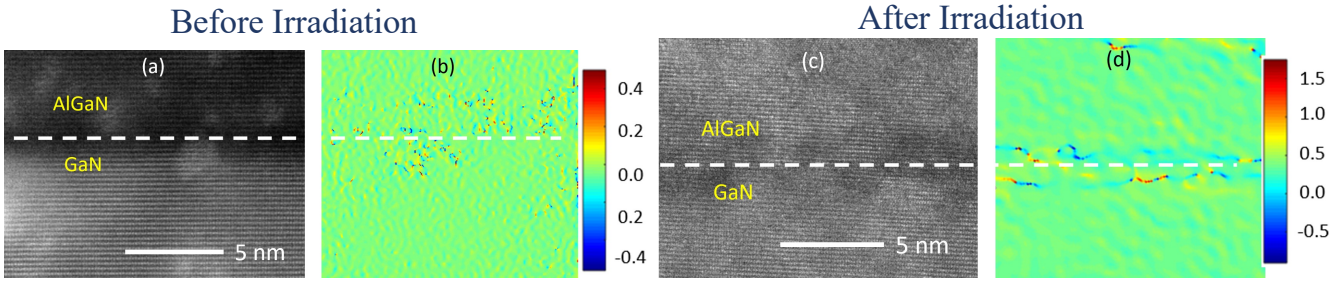


Custom In-Situ γ-ray Mrad Dose Testing Penn State RSEC Facility



PSU Collaborators: Prof. Aman Haque

HRTEM and GPA analysis before and after γ-ray irradiation



Conclusions

- PSU has significant strengths in new materials, especially in “silicon adjacent technologies” that can form the core of responses to multiple agencies via the CHIPS act
- The core facilities are a major asset, with significant potential for expansion and workforce development
- The University also has strengths in new semiconductor device development, circuit modeling, and systems architecture
- More information is needed for efforts that weren’t captured in this short overview
  - Areas where we can point to critical mass, robust coupling to industry, or strengths in workforce development are most likely to resonate with funders
  - Please respond to the forthcoming RFI

Transforming Happy Valley into Happy Silicon Valley
A Vision for Rethinking & Reimagining Semiconductor Packaging

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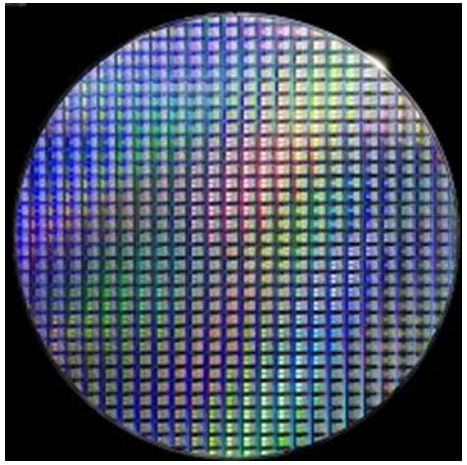
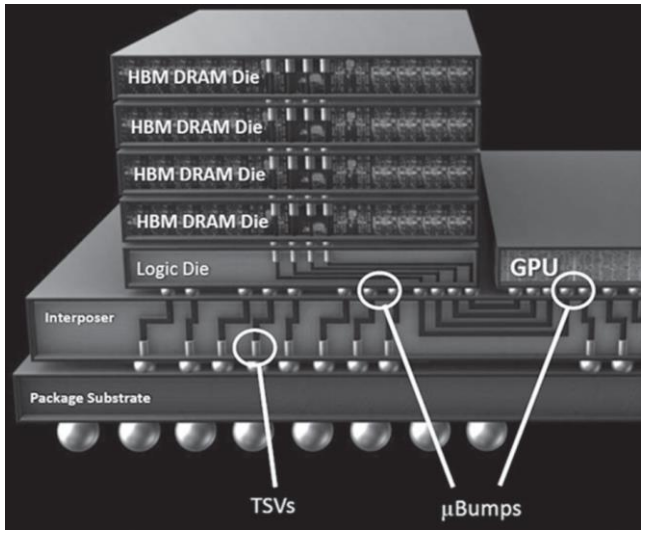
Director, CHIMES (an SRC JUMP 2.0 Center)
The Pennsylvania State University
Emeritus Professor, ECE & MSE, Georgia Tech
Former Director, 3D Systems Packaging Research Center (NSF-ERC), Georgia Tech

What is Semiconductor Packaging?

TRANSISTORS



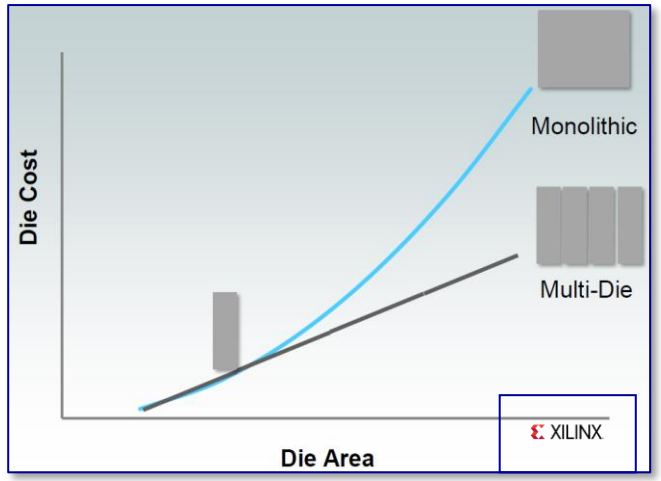
PACKAGING

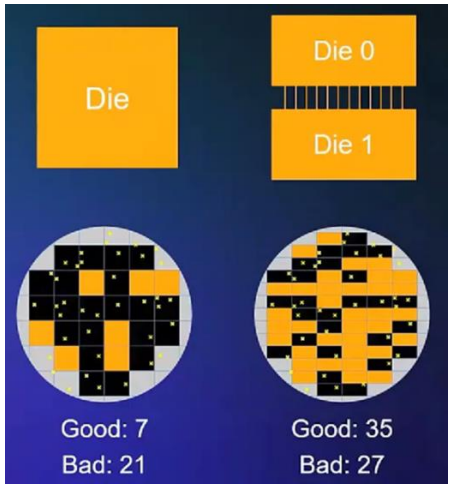


- ❑ Transistors (and chips) require packaging to communicate.
- ❑ Packaging connects chips to each other and to the external world through signaling, powering, cooling, and protection.
- ❑ <u>Electronic System = Chips + Packaging</u>

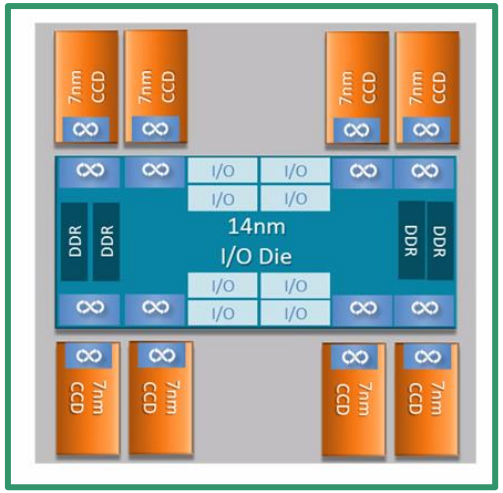
Packaging & The Next Moore's Law

Use of smaller dies from advanced nodes



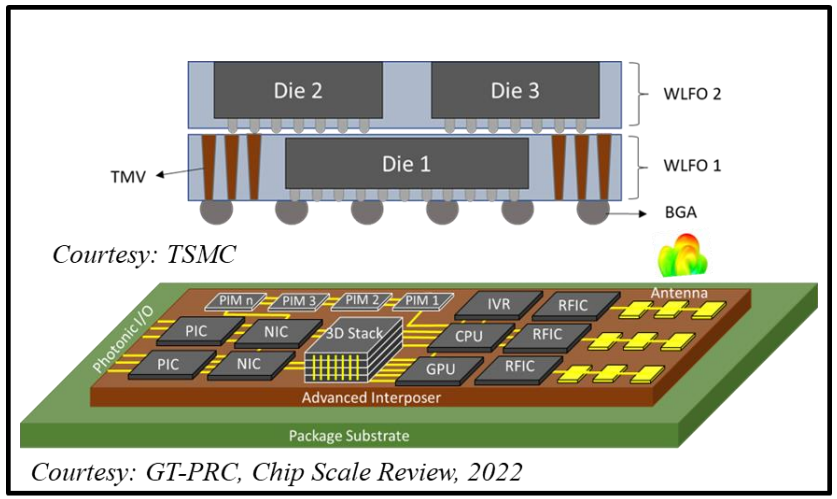


Shorter design time



Courtesy: AMD

Heterogeneous Integration



Three reasons why Packaging is becoming critical for the continuation of Moore's Law:

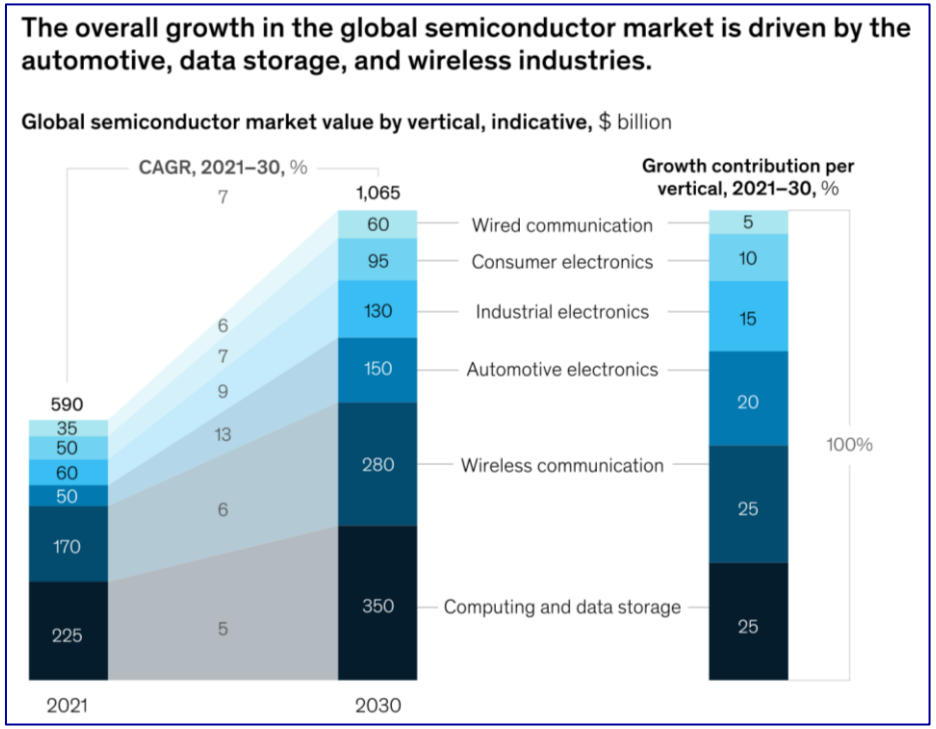
1. Higher yield using smaller dies in advanced nodes.
2. Shorter time to design with smaller dies from optimized legacy technology nodes with enhanced functionality.
3. Move towards **HETEROGENEOUS INTEGRATION**.

Why is Packaging of National Importance to US?

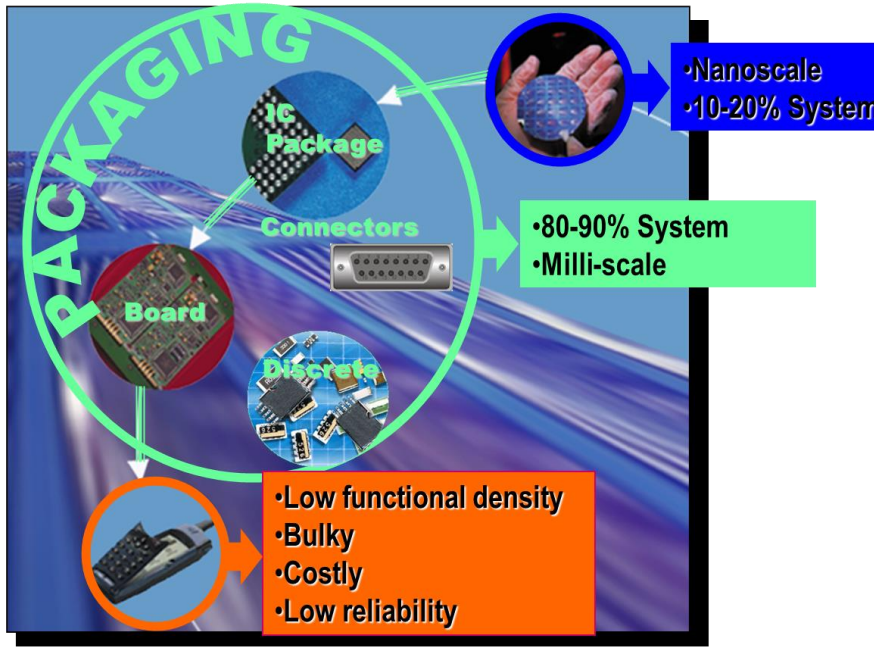
- Global semiconductor industry projected to become a trillion-dollar industry by 2030 (Source: McKinsey & Company)
  - 55 years to become a 0.5T industry
  - Expected to double in the next 10 years
  - Drivers: Computing/Storage, Wireless, Automotive, ….

- US losing Leadership
  - Chip
    - Less than 12% of Semiconductor Manuf. in USA
  - **Packaging**
    - **Less than 2% of Substrate Manuf. in USA**
    - **Less than 6.5% of Flip-Chip bumping in USA**

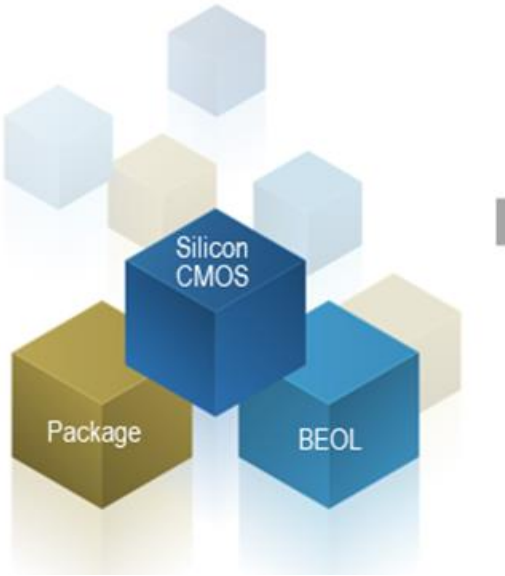
- 2022: CHIPS for America Act
  - Establish Onshoring Capabilities and U.S. Leadership
  - $52B Investment **($11B for R&D & Workforce Development)**



Rethinking & Reimagining Packaging to Establish US Leadership



Packaging (Past)



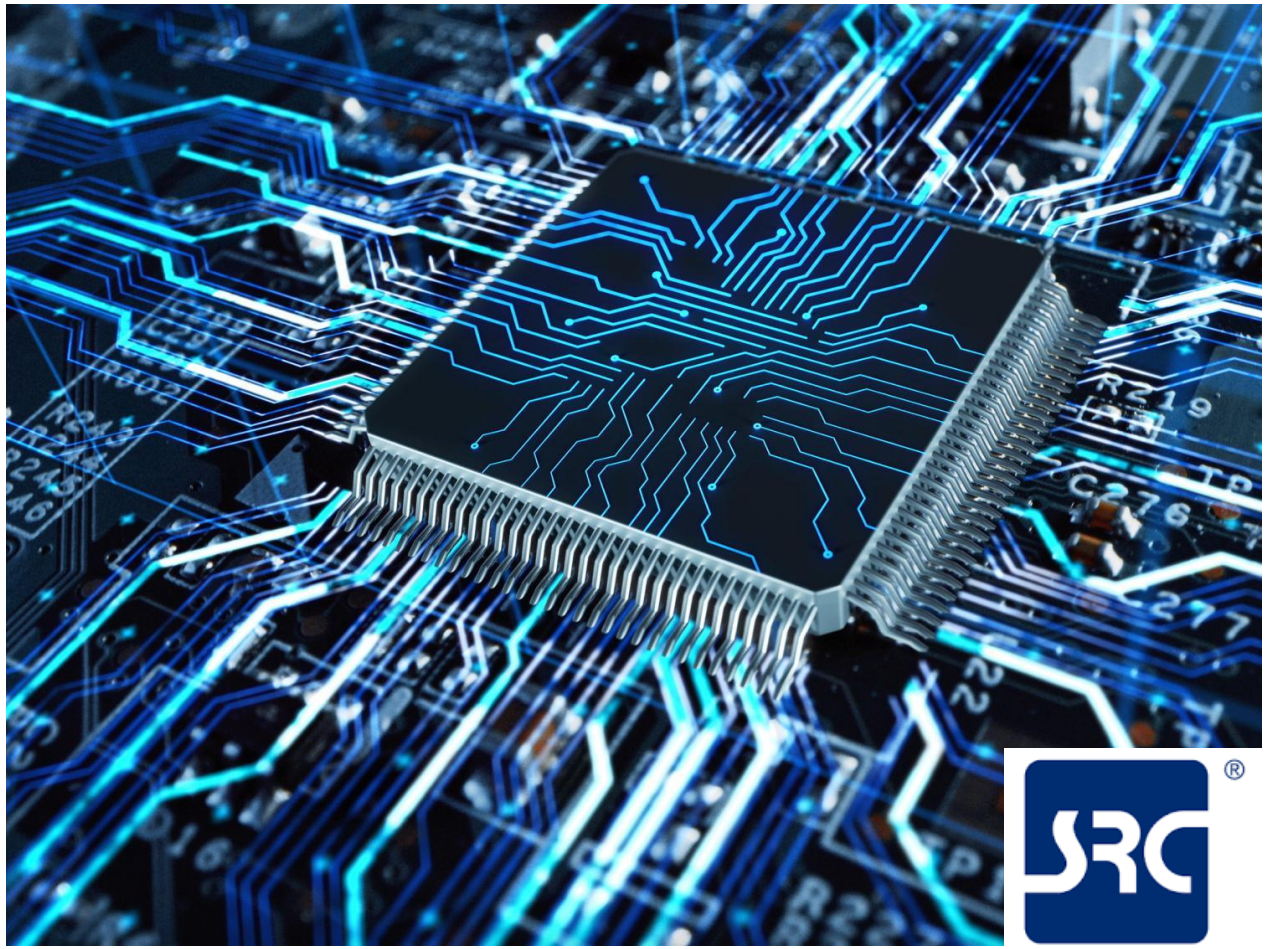
Advanced Packaging (Present)

Heterogeneous Integration (Future)

- **Past/Present:** FEOL Transistor, BEOL Wiring & Package individually developed and combined
- **Future:** New and transformative packaging technologies that overcome the slowdown of traditional dimensional scaling of systems by interconnecting a **diversity of chips, blurring the line between what is on-chip and what is off-chip, with a focus on transitioning these technologies into manufacturing**.

Introducing JUMP 2.0 Center @ Penn State (14 Univ. Partners)

Penn State leads semiconductor packaging, heterogeneous integration center



- Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES)
- Supported by the Semiconductor Research Corporation (SRC)'s Joint University Microelectronics Program 2.0 (JUMP 2.0), a consortium of industrial partners in cooperation with the Defense Advanced Research Projects Agency (DARPA)

https://www.psu.edu/news/engineering/story/penn-state-leads-semiconductor-packaging-heterogeneous-integration-center/

Next Steps ….

- Opportunities for packaging through CHIPS Act:
  - National Semiconductor Technology Center (NSTC)
    - Includes packaging but unclear up to what extent.
  - **National Advanced Packaging Manufacturing Program (NAPMP)**
  - **Manufacturing USA Institutes** (3 Institutes w/ one expected in Packaging)

		YEAR 1	YEAR 2	YEAR 3	YEAR 4	YEAR 5	
9906(c)	NSTC	$2B	$2B	$1.3B	$1.1B	1.6B	-
9906(d)	NAPMP	$2.5B					
9906(e)	NIST Metrology	$500M					
9906(f)	Manufacturing USA Institute						

National Advanced Packaging Manufacturing Program (NAPMP)

Game Plan:

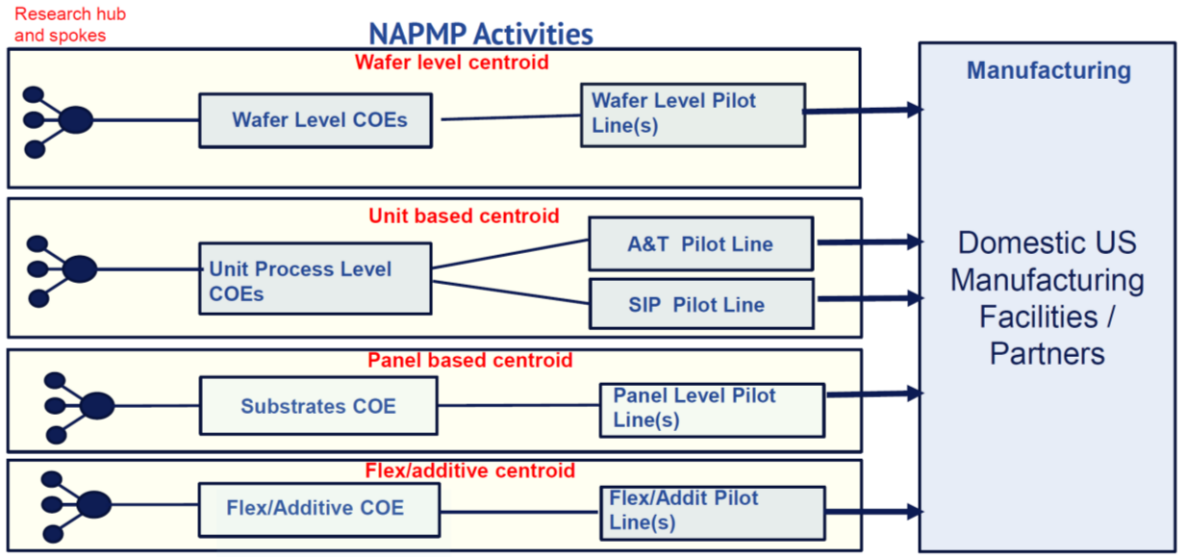
1. Intel and/or IBM (www.asicoalition.org) are expected to lead a major coalition
   - Hub & Spoke model being proposed feeding into pilot lines and manufacturing facilities
   - Become part of the team. Visits by Intel & IBM to Univ. Park (Mar/Apr)
2. Form National University Center of Excellence (UCE)
   - Discussions ongoing with PSU, Purdue, MIT, RPI, & SUNY

NAPMP Target Areas

CHIPS for AMERICA

Technology innovation	Create an R&D environment advancing the state-of-the art in advanced packaging.
Ecosystem support	Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.

Source: Eric Lin, Interim Director, CHIPS Research and Development Office, NIST

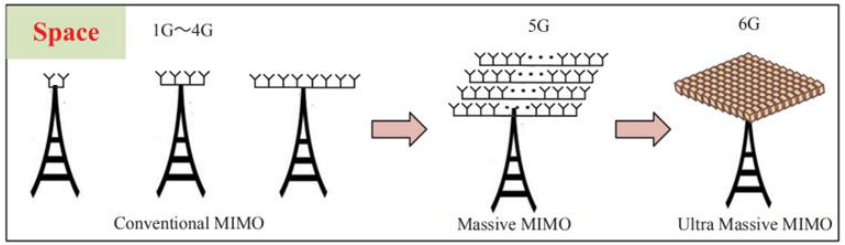


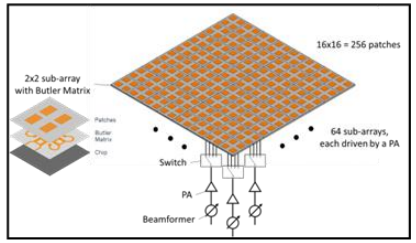
www.asicoalition.org

Manufacturing USA Institute (MI) on Packaging

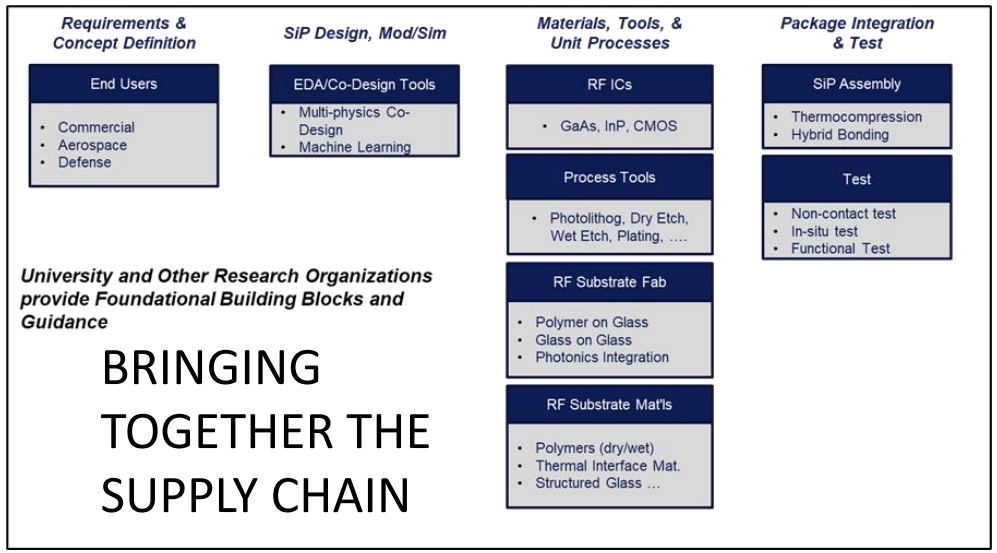
One Possibility:

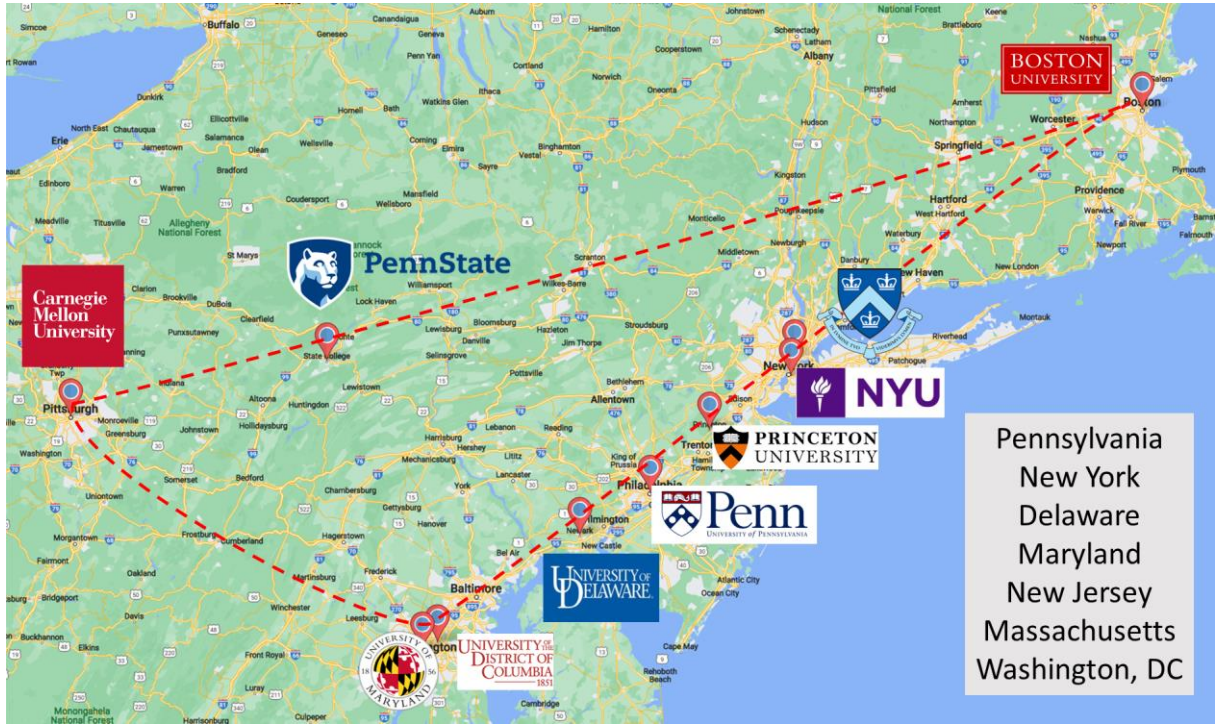
- ❑ Institute Focused on Advanced Packaging for Advanced Communications
- ❑ Request for Information (RFI) submitted to NIST (https://www.regulations.gov/comment/NIST-2022-0002-0069 Total submissions=94)
- ❑ Include partner universities from the Mid-Atlantic HUB
- ❑ Focus on Wafer Level Glass Packaging (Research from UCE transitioned into prototyping)





- Penn State
- GaTech
- Qorvo
- 3DGS
- AMAT
- Schott
- Menlo
- Corning
- Synopsys
- iNEMI
- Boeing
- Absolics
- GWU





Moving Forward - Building an Ecosystem @ Penn State

Engineering Science & Mechanics

Materials Science & Engineering

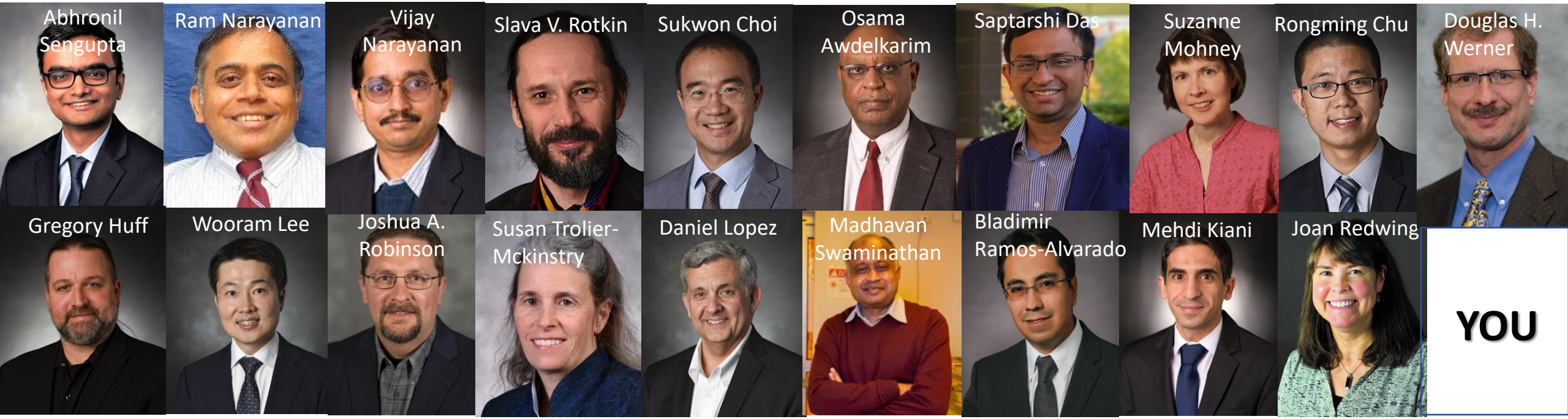
PennState Materials Research Institute

Mechanical Engineering

Electrical Engineering

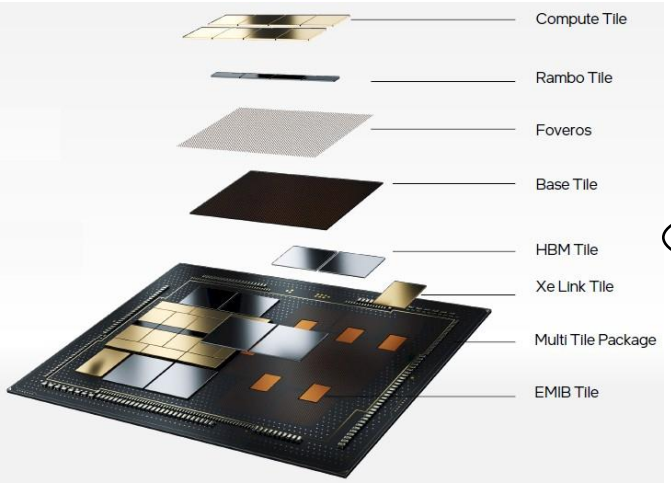
Computer Science & Engineering

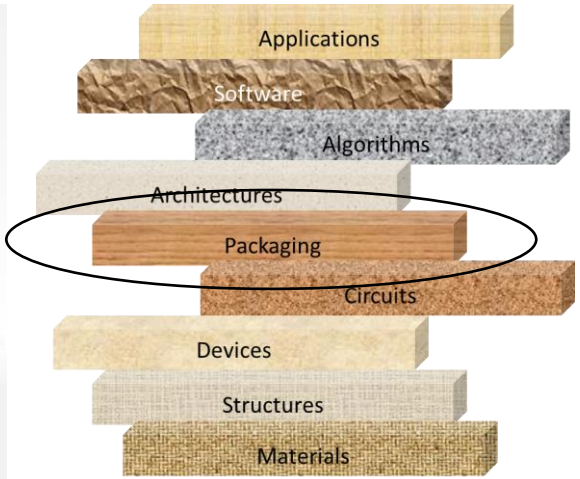
- NEMS, photonics, optoelectronics, electronics
- Electro-thermal co-design & thermal management
- Device & System reliability
- HI & 3D Integration
- Biomedical systems integration & packaging
- III-V & 2D materials on Si
- Widegap semiconductors for harsh environment
- Multi-functional RF integrated systems
- mmWave phased arrays & antenna integration
- ALD for ultra-low k dielectrics
- Dielectric, piezoelectric, and ferroelectric
- Power aware AI hardware
- Neuromorphic computing
- Heat Transfer Modeling
- Metasurfaces for Electronics & Photonics
- Wafer & Panel scale packaging

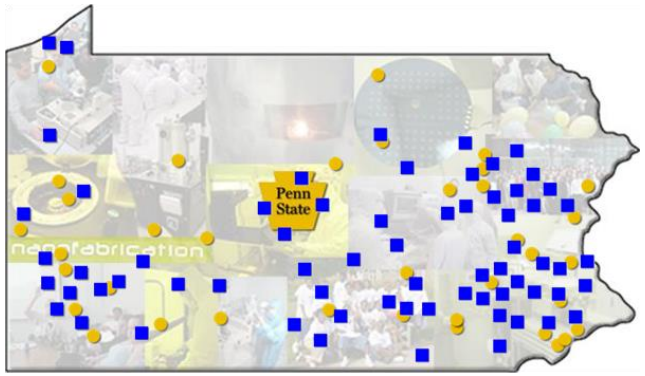


Penn State & Semiconductors in 10 Years – Just Imagine!

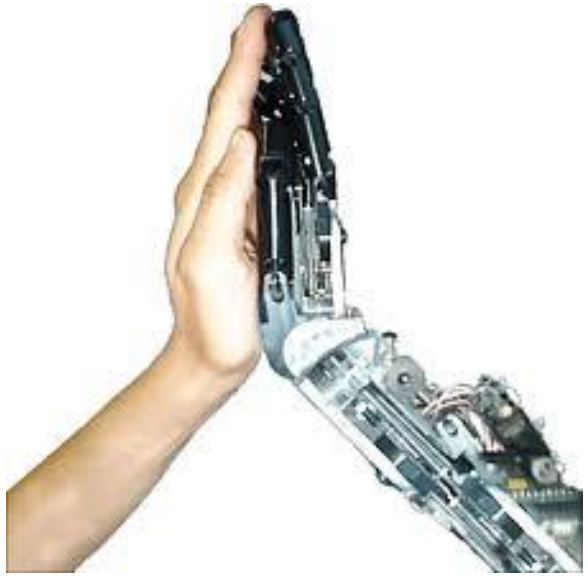
- Active semiconductor R&D across the commonwealth from Materials-to-Applications where Emerging Applications and Future Systems serve as the driver for research into adjacent silicon technologies that use diverse materials on a silicon platform supported by dense connectivity between chips.
- An eco-system with 100+ companies and several govt. labs working closely with Penn State researchers in a pre-competitive environment, providing mentorship and enabling commercialization.
- Translational research facilities on campus with low volume manufacturing capability providing access to DoD, Start-ups and other agencies.
- Penn State students being sought after worldwide for semiconductor related jobs due to industry relevant education that combines technology, business, and hands on experience.
- A self-sustaining environment for fundamental, applied, and translational research in semiconductors.







Courtesy: Osama Awadelkarim, Penn State



We need your feedback!

https://forms.office.com/Pages/DesignPageV2.aspx?subpage=design&FormId=RY30fNs9iUOpwcEVUm61LswR68uNzRBGuAVaCdYfQF5URFNDQ0ZCUk1NNDg3UUVCT1RORlFZS0owTS4u&Token=720a479bb50546008f1c9472a9b1fe22