The Pennsylvania State University

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THE RELIABILITY OF THE SILICON NITRIDE DIELECTRIC IN CAPACITIVE MEMS SWITCHES

A Thesis in

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by

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ABSTRACT

Silicon nitride thin film dielectrics can be used in capacitive radio frequency micro-electromechanical systems switches since they provide a low insertion loss, good isolation, and low return loss. The lifetime of these switches is believed to be adversely affected by charge trapping in the silicon nitride. These charges cause the metal bridge to be partially or fully pulled down, degrading the on-off ratio of the switch. Little information is available in the literature providing a fundamental solution to this problem.

Consequently, the goals of this research were to characterize Si_xN_y–based MIM (Metal-Insulator-Metal) capacitors and capacitive MEMS switches to measure the current-voltage response. It was hoped that in this way it would be possible to describe the mechanisms responsible for the conduction and trapping behavior, as well as to estimate the potential barrier heights (Poole-Frenkel and Schottky). All of the silicon nitride films were deposited by low pressure chemical vapor deposition at temperatures <250°C.

Accordingly, different top electrodes, –Al, Pt, or Au-Ti were fabricated by the lift-off/metal sputtering process on wafers with Si_xN_y /Ti-Au /Si_xN_y/Si structures. The upper Si_xN_y layer was removed by the reactive ion etching process (RIE) at four or more locations on the wafer in order to provide contact paths to the bottom electrode. The silicon nitride films consisted of two different compositions (Si-rich and near stoichiometric).

The leakage currents of MIM structures were then were studied at room temperature (25^oC) over a wide range of electric fields (0-4MV/cm) for the three different top electrodes. In the near-stoichiometric films, a dependence of the leakage

current on the electrode was observed for both voltage polarities up to the highest electric field of 4 MV/cm. The polarization currents were extremely long-lived in these samples (>3600 seconds), and thus steady-state currents couldn't be achieved at the studied fields (<4MV/cm). The magnitude of these currents was the largest for the Pt, the smallest for the Al, and intermediate for the Ti-Au top electrodes.

It was concluded that the Poole-Frenkel mechanism dominated the conduction in the Si-rich silicon nitride films at high fields (> 1MV/cm). The high frequency dielectric constant was calculated to be 3.67±0.04 for the Si-rich composition with Ti-Au electrodes. Additionally, the Poole-Frenkel potential barrier height was found to be 0.83±0.014eV with a pre-exponential factors (C) of $2.52(\pm 0.154)\text{x}10^{-4}$ $AV^{-1}m^{-1}$ at an electric field of 2.32MV/cm.

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Chapter 1

Introduction

Microelectromechanical systems (MEMS) capacitive switches have been of great interest as replacements for conventional semiconductor switches. Although capacitive switches can be made quite small, and provide low insertion loss over wide frequency ranges, the reliability of these devices still needs to be improved.[1] One of the problems that continues to exist in the widely-used Si_xN_y dielectrics of these devices is charge trapping, which results in stiction. Studying the charge transport phenomena in the MIM (metal-insulator-metal) capacitor is a practical approach to investigating the charge trapping problem. Of particular interest is whether or not changes in the dielectric deposition conditions of contact metals can mitigate the reliability issues.

Charging currents of the MIM capacitor as a function of the time consist of transient currents and leakage currents. Distinguishing between these two currents is crucial to studying conduction mechanisms in silicon nitride dielectrics. Consequently, techniques, such as the Curie-von Schweidler law and pulse mode were utilized to eliminate these difficulties.

Current transport across an insulator doesn't necessarily depend only on the insulator material, but can also be a function of the metal work function. Using different metal electrodes with different work functions such as Au, Al, and Pt can change the current flow in the dielectric if the injection is controlled by a Schottky barrier. Conduction in the insulator may also arise by trapping and detrapping of charges in the bulk of the dielectric, which is described by the Poole- Frenkel mechanism.

A major goal of this thesis was to investigate charge trapping in the silicon nitride dielectric of capacitive MEMS switches via the study of the current transport in MIM capacitors. To accomplish this objective, the conduction mechanisms were studied to understand the mechanisms governing leakage currents in the dielectric. Two types of silicon nitride films, one near stoichiometric, the other silicon rich, were investigated. Self-consistency of the proposed conduction mechanisms was pursued by checking the optical frequency dielectric constants, as well as the potential barrier heights. The following chapters present relevant background information on both MEMS capacitive switches and silicon nitride dielectrics. They also describe the experimental processes by which the films were prepared and characterized, as well as a discussion of the measured experimental results.

1.1 References

1 C. Goldsmith, J. Kleber, B. Pillans, D. Forehand, A. Malczewski, and P. Frueh, "RF MEMS: Benefits & Challenges of an Evolving RF Switch Technology," in IEEE GaAs Dig., 147-48 (2001).

Chapter 2

Literature Review

2.1 Introduction

The objective of this study was to better understand the origin of the stiction problem associated with charge trapping in the silicon nitride dielectrics used in capacitive MEMS switches, and gain insight into the conduction mechanisms governing this behavior. Thus, this chapter provides a brief review of capacitive MEMS switches with a focus on charge trapping in the dielectric materials, and the background information related to carrier transport within silicon nitride dielectrics.

2.2 RF Capacitive MEMS Switches Motivation and Applications

Micro-Electro-Mechanical Systems (MEMS) technology has grown rapidly in recent years. As an example of this technology, RF (Radio frequency) capacitive MEMS switches are emerging as possible replacements for conventional semiconductor switches.[1] In comparison to semiconductor switches (FET-Field Effect Transistor and PIN-diodes), RF capacitive MEMS switches exhibit significant advantages, such as a low insertion loss (<0.1dB at 40GHz), good isolation (<35dB at 40GHz), low return loss, low cost, and low power consumption.[1-2] RF MEMS switches are of particular interest to the radar and wireless communication industries, as replacements for power-hungry semiconductor-based switches.[3] Figure 2.1 shows examples of capacitive switches at the micron scale.[4]

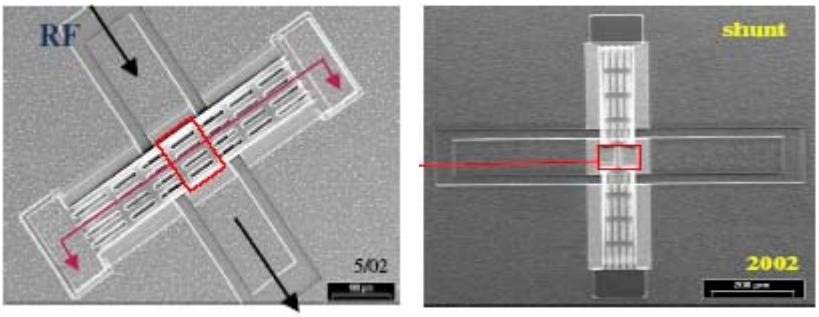

Figure 2.1 Microphotographs of some capacitive MEMS switches.[4]

Specific application of these switches can be found in phase shifters, tunable band filters/matching networks, and reconfigurable phased arrays antennas.[3] Each of these is briefly summarized in the following paragraphs.

Conventional electronic phase shifters are typically made on GaAs and utilize the MESFET (Metal-Semiconductor-Field-Effect-Transistor) or pHEMT (High Electron Mobility Transistor) as typical semiconductor switches.[5] These components control connections to low and high pass filters to accomplish the needed phase shift.[6] As switching components, these switches show a higher loss compared to RF MEMS capacitive switches.[2] The typical loss of a Ka-band (26.5 - 40GHz) 4-bit phase shifter obtained using a pHEMT is nearly 6.5dB.[5] Conversely, RF MEMS capacitive switches have already shown a low loss (<0.1dB) at 40 GHz.[2] Applying these switches to Ka-band, or X-band phase shifters would decrease one of the main losses in conventional phase shifters and thereby significantly lower the overall RF loss in phase shifters.[6] Reducing the loss in the array phase shifter decreases the cost, weight (and size) as well as the heat dissipation by enabling use of a smaller number of amplifiers.[5-6] Figures 2.2(a-b) shows 2-bit phase shifters as circuit components.[7]

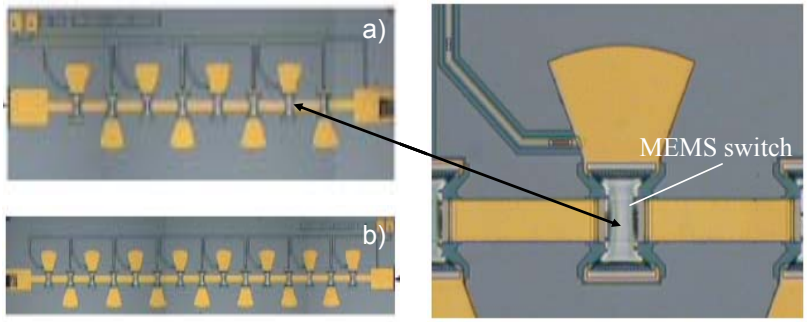

Figure 2.2 a) Photograph of 2-bit 90º MEMS phase shifter as a circuit component **b)** Photograph of 2-bit 180º MEMS phase shifter as a circuit component.[7]

MEMS capacitive switches have also been used in tunable filters and tunable matching networks. In tunable filters, since MEMS switches are variable capacitors, they can be utilized in a DMTL (distributed MEMS transmission line) to work with tunable resonators by changing the frequency of the center transmission line through loading capacitance, thus yielding phase shifts[8] (see Figure 2.3). In these systems, DMTL tunable resonators with capacitive switches have been shown to provide a 3.8% tuning range at 20GHz with 3.6dB insertion loss.[9]

Another important application of MEMS capacitive switches is in reconfigurable phased arrays antennas for wide-band operation. By utilizing capacitive switches, multi-band antennas can be reconfigured within microseconds to provide different applications at detached frequency bands.[10] In this application, PIN diodes and FET switches fail due to the narrow bandwidth arising from their non-linear characteristics.[11] Figure 2.4 shows a photograph of an antenna integrated with RF MEMS switches. As shown in the figure, turning the capacitive switches on/off enables activation of a single antenna (A1-first antenna, A2-second antenna, or A3-third antenna) or more than one antenna to generate a radiative patch for reconfigurability.[12] In this system, MEMS switches offer very low loss

(0.1-0.2 dB) in the on state and high isolation in off state (25-35 dB) at 40 GHz.[11]

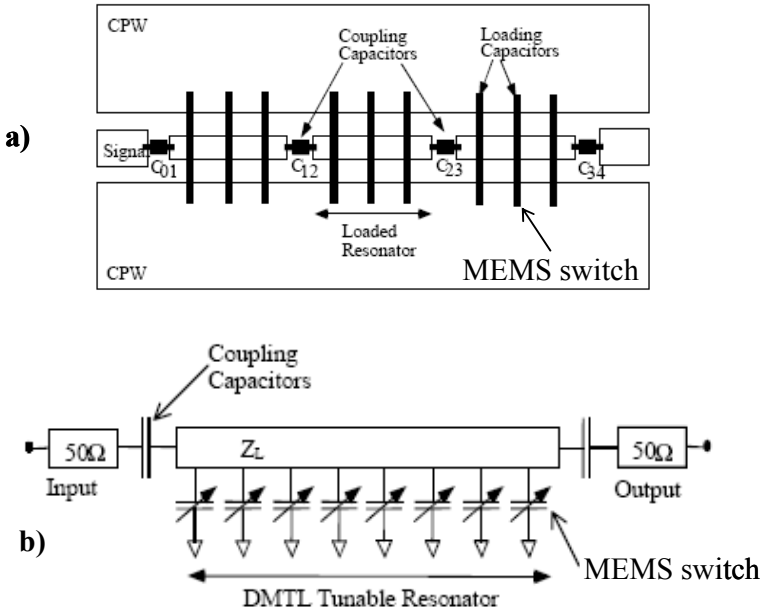

Figure 2.3 MEMS capacitive switches with a DMTL-based tunable resonator **a)** Top view **b)** Equivalent circuit model.[8]

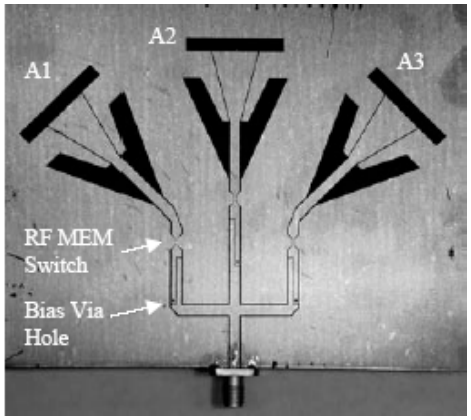

Figure 2.4 Photographs of several antennas integrated with RF MEMS switches. A1, A2, and A3 are the first, second, and third antennae, respectively.[12]

2.3 Capacitive MEMS Switches Operation and Parameters

A capacitive MEMS switch consists of a thin metal membrane (typical length=200-300 µm and width=20-140µm) suspended over the center conductor of a coplanar waveguide (CPW) (width=100-160µm) that passes RF signals, and a thin dielectric layer (thickness=0.1-0.3 µm) that isolates the center conductor from a metal bridge.[13] The capacitive bridge is suspended over CPW and grounds are equally spaced (20-60µm) from a center conductor line.[13] The air gap (height=1.5-2µm) resides between the dielectric surface and the membrane. Figure 2.5 (a-b) shows an example of a typical capacitive switch from the side and top view.[14]

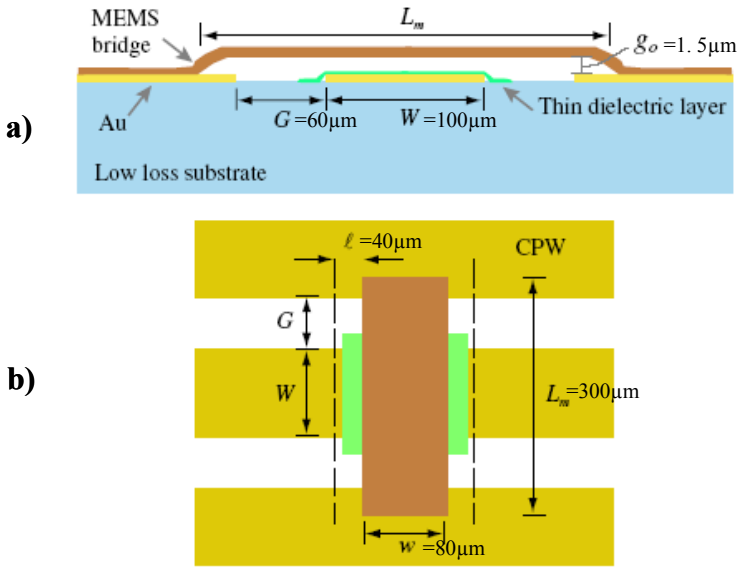

Figure 2. 5 a) The cross section of a typical capacitive switch in the up position **b)** Top view of the switch. L_m is the membrane length from the CPW ground plane edge, g_o is the membrane height, W is the CPW center conductor width, G is a space between CPW, ℓ is the distance from the reference plane to the edge of the bridge, and w is the bridge width.[14]

Electrically, capacitive switches are variable capacitors that have two states (on and off).

When the switch is actuated (on-state) by applying a DC bias between the center conductor and a metal bridge, electrostatic forces between the dielectric surface and the metal bridge pull the bridge into a down position.[13] Figures 2.6 (a-c) illustrate the up and down state of a capacitive switch and equivalent circuit models.[8,14]

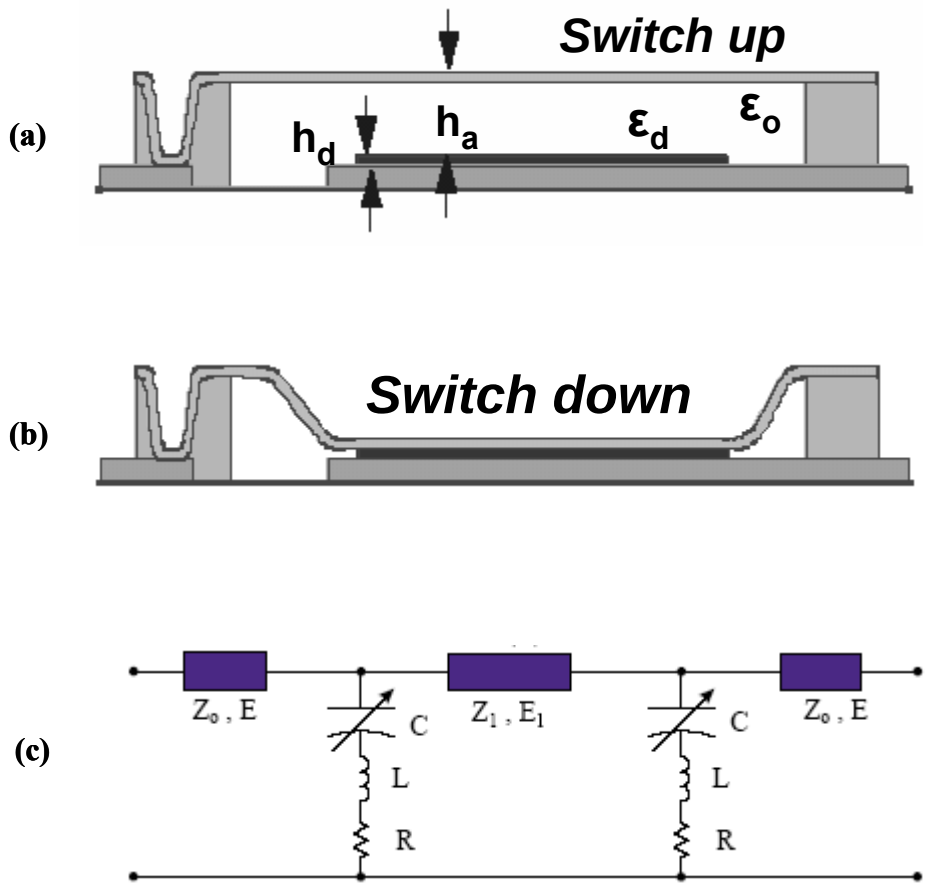

Figure 2.6 Capacitive switches **a)** In the up state (off) **b)** In the down state (on) **(c)** Equivalent circuit model for the two MEMS bridge capacitive switch. Z_o is the port impedance, Z_1 is the midsection line impedance, C is the bridge capacitance, L -R are the inductor-resistor of the switch, and E_1, E_o are the electrical element of the midsection and port impedance, respectively.[8,14]

The pull-down voltage due to electrostatic forces is given by[13]

$$V_p = \sqrt{\frac{8kg_o^3}{27\varepsilon_o W\omega}} \qquad (2.1)$$

where k is the effective spring constant of the membrane, W is the width of the CPW center conductor, ω is the membrane width, ε_o is the permittivity of free space, and g_o is the nominal gap height between the membrane and the dielectric surface. When the DC bias is removed (off-state), the mechanical stresses in the metal bridge overcome the stiction forces tending to hold it down, and return the bridge to the original position.[14] The capacitive switch provides different capacitance values in the on and off states. Depending on the operation voltage (20-50V), the up-state and down-state capacitance for typical switches were reported to be 30-35fF and 3-4pF, respectively.[13,14] As shown in Figure 2.7, the capacitance of the capacitive switch changes as a function of applied voltages between on and off state cycle hysteretically.[15] When the switch is unactuated, it exhibits the minimum capacitance value due to the air gap between the dielectric and the bridge.[13]

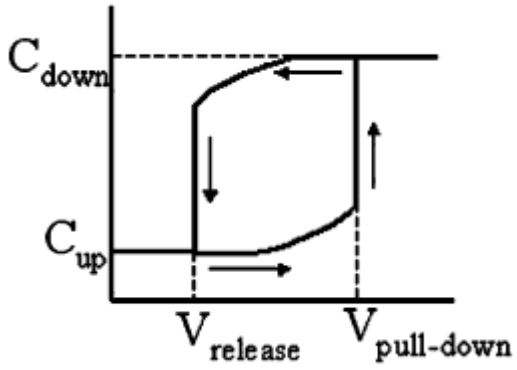

Figure 2.7 Capacitance as a function of the applied voltage shows a hysteresis during pull-down and release of the capacitive switch.[15]

The up-state capacitance (off-state) of the switch can be found by[16]

$$C_{up} = \frac{1}{\frac{h_d}{\varepsilon_d A} + \frac{h_a}{\varepsilon_o A}} \qquad (2.2)$$

where h_d is the dielectric layer thickness (In order for a typical dielectric such as Si_xN_y to survive actuation voltages of 20-50V, a dielectric layer thicker than 1000Å is preferred)[14], h_a is the height of the air gap between the bridge and the dielectric, and ε_d, ε_o are the dielectric constants of the dielectric material and the air, respectively. A is the overlap area between the bottom electrode and the membrane. When the switch is actuated, it exhibits the maximum capacitance value. Ideally, the down-state (on-state) capacitance can be found by[16]

$$C_{down} = \frac{\varepsilon_d A}{h_d} \qquad (2.3)$$

In a typical switch, the geometry of the capacitive bridge and CPW is designed to reduce the electrical resistance in order to accomplish the on-off capacitance that enables impedance matching of the system.[14] In particular, the on-impedance of a switch at high frequency is affected by parasitic resistances.[14,16] Consequently, the performance of the switch is limited by its cut off frequency. This frequency is given by[16]

$$f_c = \frac{1}{2\pi C_{off} R_{on}} \qquad (2.4)$$

where R_{on} is the effective on-state resistance and C_{off} is the off-state capacitance of the switch. The important figure of merit for quantifying the switch performance is the down/up capacitance ratio (C_{down}/C_{up}), which must be as high as possible.[16]

In order to achieve the best switching performance, the off capacitance (C_{up}) is required to be as low as possible (low insertion loss) and the on capacitance (C_{down})

should be as high as possible (high isolation).[13,16] This figure of merit for a capacitive switch is given by[13]

$$\frac{Z_{down}}{Z_{up}} = \frac{C_{down}}{C_{up}} = \frac{\varepsilon_o h_d + \varepsilon_d h_a}{\varepsilon_o h_d} = 1 + \frac{\varepsilon_d h_a}{h_d} \qquad (2.5)$$

where Z_{down} is the on-state impedance and Z_{up} is the off-state impedance of the switch. As seen in this formula, the high on-off ratio can be achieved by choosing a material with high dielectric constant, decreasing the dielectric layer thickness (limited by pin-holes and breakdown field), or increasing the nominal air gap height (limited by pull-down voltage). For conventional designs, this value is reported to be in the range between 50 and 150.[16] However, on-off capacitance ratios bigger than 100 are desired for switching signals at microwave frequencies.[13] The capacitive switch developed by Texas Instruments, Dallas, TX (now a part of Raytheon) provided on-off capacitance ratios between 60 and 100.[17] The fabricated switch dimension was 120μm in width and 280μm in length, and used an Al alloy bridge. As a dielectric layer 0.2μm thick PECVD silicon nitride (ε=6.7) was deposited on top of the center conductor. The typical switching time was on the order of 3.5↓-↑5.3μs with an actuation voltage of 50V. Insertion losses in the up-state were 0.15 dB at 35 GHz and 0.28dB at 35 GHz. Isolation was 15 dB at 10GHz and 5dB at 35 GHz. A switch lifetime of 500 million cycles has been demonstrated. Table 2.1 summarizes the characteristics and performances of RF switches fabricated by different companies and institutions.[19] The capacitive switch made by the University of Michigan showed an on-off capacitance ratio of ~60-120 for a capacitance area of 80x100μm^2 with nominal air gaps of ~0.8 and1.5μm, respectively.[14] As an isolation layer, 100nm thick PECVD Si_xN_y (ε~7.6) was deposited on top of the Ti-Au center

conductor. The overall insertion loss and isolation achieved were 0.4-0.6 dB at 22-38 GHz and 40-50dB at 22-35 GHz, respectively.

Table 2.1 Characteristics and performance of RF MEMS switches made by different companies and institutions.[19]

Device characteristics and performance parameters	FET switch	Rockwell (RSC) [16, 26]	Raytheon/TI [28–30]	HRL Labs [19–20]	University of Michigan [27]
MEMS technology	—	Surface	Surface	Surface	Surface
Device size (μm × μm)	~1 mm^2	80 × 160	120 × 280	~120 × 300	~1000 × 2000[a]
Current handling (mA)	~200	200	Not available	140	Not available
Structural material	GaAs	SiO_2	Al alloy	Si_xN_y	Plated Au
Actuation mechanism	—	Electrostatic	Electrostatic	Electrostatic	Electrostatic
Actuation voltage (V)	~1	~60	~50	~25	15–20
Contact mechanism	Semiconductor	Au based metal	Capacitive	Au	Capacitive
Insertion loss (dB)	2 at 6 GHz	0.2 (dc–40 GHz)	0.15 at 10 GHz 0.28 at 35 GHz	0.2 (dc–40 GHz)	0.6 (22–38 GHz)
Isolation (dB)	−22 at 2 GHz −20 at 6 GHz	−32 at 10 GHz −22 at 40 GHz	−15 at 10 GHz −35 at 35 GHz	−40 at 12 GHz −27 at 40 GHz	−40 at 22 GHz −50 at 35 GHz
Switching time	10 ns	2–5 μs	3.5–5.3 μs	20 μs	Not available
Lifetime (million cycles)	>100 000	~100 (cold) 10s (hot 1–40 mA)	500	~4 (hot 10 mA)	Not available
Others	Values may vary from device to device	third order IM product 71.5 dB below tone level	IP3 > +66 dBm	Unidentified resonance at 8.5 GHz	Tuned for 30 GHz performance

Device characteristics and performance parameters	Northeastern University [21–23]	Siemens AG [24]	OMRON [31]	NEC Corporation [25]
MEMS technology	Surface	Bulk	Bonded wafer	Bonded wafer
Device size (μm × μm)	Beam = 30 × 65	1.5 (mm^2)	2000 × 2500	250 × 900
Current handling (mA)	150	>100	Not available	Not available
Structural material	Au/Ni	Silicon epi	Silicon	P++ Silicon
Actuation mechanism	Electrostatic	Wedge electrostatic	Electrostatic	Electrostatic
Actuation voltage (V)	30–300	24	16–19	125
Contact mechanism	Au	Plated Au alloy	Au	Au
Insertion loss (dB)	Not available dc R ~ 0.1–10 Ω	Not available dc R < 5 Ω[b]	Not available dc R ~ 0.5 Ω	0.2 at 30 GHz
Isolation (dB)	Not available	Not available dc R > 100 GΩ	Not available	−13 at 30 GHz
Switching time	150 kHz cutoff	<0.2 ms	<0.3 ms	—
Lifetime (million cycles)	0.01–1000[c] (cold)	Not available (mechanical life 100)	1–10 (hot 10mA)	—
Others	500 million cycles for N_2 packaged hot-switch at 10 mA	Contact force is of the order of 1 mN	5 mN contact force Lifetime uses resistive load w/10 V	Double-hump design is used above

[a] Including four membrane switches to form a cross switch with short transmission lines.
[b] Including feed line resistance.
[c] Cold-switching lifetime depends on number of contacts ranging from 8 to 64.

The capacitive switch made by MIT Lincoln Laboratory, Lexington, MA had an on-off capacitance ratio of 141 (on-capacitance-1.2pF, off-capacitance 8.5fF).[18] The capacitive switch consisted of 150nm thick SiO_2 (ε=3.9) on a Pt-coplanar center line and a Pt-capacitive bridge with a contact area of 46x148μm^2. The device had an insertion loss of 0.5 dB at 5GHz and 0.7dB at 40GHz. The switching speed for this device was slow (3↓-↑20μs). However, a switch lifetime of 10^9 cycles was demonstrated without failure. In addition, it was proposed that high-*k* dielectric materials should provide better on-off capacitance ratios and lower actuation voltages than low-*k* materials.[8] For instance, the LG Corporate Institute of Technology, Seoul, Korea presented an on-off capacitance ratio of bigger than 600 using capacitive switches with a 190nm thick $SrTiO_3$ (ε=~30-120) isolation layer.[16] The devices consisted of ~2.5-3.5μm air gap and a capacitance area of 100x100μm^2. Addionally, the switch operation resulted in low insertion loss of 0.08 dB at 10 GHz and high isolation of 42 dB at 5 GHz. The over all actuation voltages varied between 8 and 15 volts.

2.4 Device Reliability

One of the factors limiting implementation of capacitive switches is the limited switch lifetime. There are several problems reported to affect the lifetime of MEMS capacitive switches, such as creep in the metal bridge, distortion in the nominal air gap, and stiction of the metal membrane to the dielectric layer.[20] Each of these is briefly summarized in the following paragraphs.

The residual stress in a metal bridge can affect the switch performance after long term deformation by means of creep.[21] Creep might be an important problem particularly

during hot switching of devices where a temperature increase can be anticipated.[20] The stresses present in the bridge can yield creep with increased temperature, permanently deforming the bridge and therefore resulting in the bridge failure.[20-21] Hence, the bridge material should be chosen carefully to minimize this effect. High melting point metal alloys (Al-Cu-Mg-Mn) have been recommended for preventing creep induced degradation in metal bridges.[22]

The nominal air gap height between the membrane and the dielectric surface might be distorted by hillocking of the metal bridge, surface roughness of the contacts, or residue left after the release etch.[19] The change in nominal air gap height degrades the on-off ratio and increases the pull-down voltage of the capacitive switch.

Hillocking might occur if a low melting temperature metallic films is heated, for example during packaging of the switches.[17] When Al is employed as a metal bridge, hillocking arises.[17] Hillocking can be solved by depositing a thin layer of a high melting temperature metal.[19] For instance, chrome might be deposited on top of the aluminum.[17] Additionally, surface roughness of contacts can prevent the two surfaces form making intimate contact in the down-state, and therefore decrease the on-capacitance of the switch.[14] The on-capacitance of the capacitive switch was reported to change from 2.1 pF to 3.5 pF for 2000 Å thick PECVD silicon nitride films with surface roughnesses (RMS) of 21nm and 6nm, respectively.[17] As shown in Figure 2.8 (a-b), when the surface roughness is increased from 0 to 100Å, the on-off capacitance ratio of Si_xN_y films drops to approximately 40% of their initial values.[14] Therefore, it is necessary that the surface roughness of the dielectric layer be below 40Å in order to obtain an efficient on-off capacitance ratio.[14]

Stiction between an insulator surface and the metal bridge can occur due to moisture, organic deposits, and contaminants, causing contact surfaces to stick to one another during operation.[21] The solid-solid and liquid-solid adhesion are due to interatomic attractions, mainly van der Waals forces and capillary forces, respectively.[20] As a solution to this problem, hermetic-0-level packing of devices is essential to avoid moisture and contaminants from migrating into the switching and pull-down region of switches.[21]

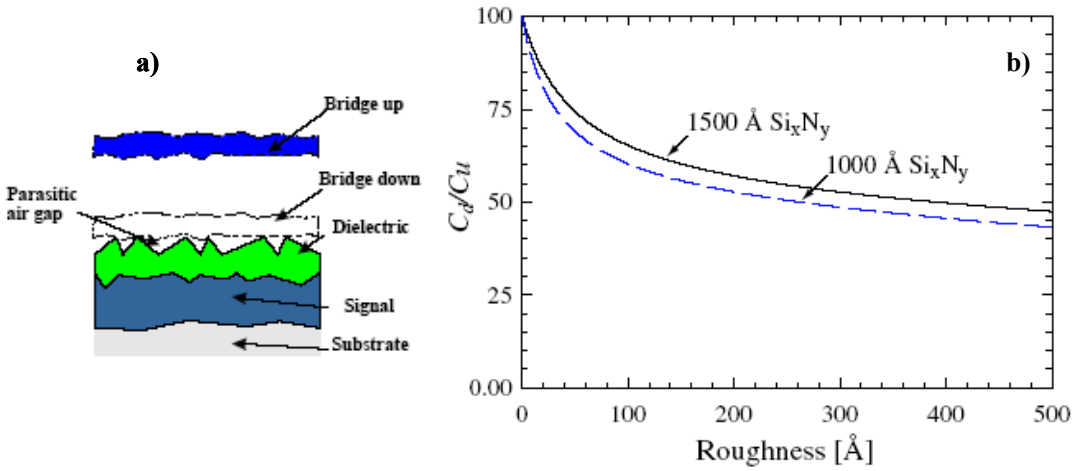

Figure 2.8 a) Schematic of a metal bridge and dielectric layer with a rough surface in the up-down state **b)** Down-up capacitance ratio changes as a function of the surface roughness.[14]

Stiction of the metal bridge to the dielectric layer due to charge trapping in the insulator is a major failure mode in capacitive MEMS switches. Hence, this thesis concentrates on charge trapping in the dielectric. When a capacitive switch is actuated, a high electrostatic field across the thin dielectric layer causes charges to build up in the dielectric.[23] These charges hold the capacitive bridge either fully (failing the switch completely) or partially (degrading the C_{on}/C_{off} ratio) in the down position when the

voltage is removed.[24] Consequently, the metal bridge can't be released unless enough time is given for the charges to relax in the system. This process can last on the order of seconds to weeks depending upon the dielectric material.[23-24] This effect is manifested as a shift of the capacitance – voltage (C-V) curve with time and cycling.[25] Figure 2.9 shows a shift of a switch C-V curve for less than 10^6 cycles. This measurement was carried out on a capacitive switch and demonstrates that the shift occurs for both positive and negative bias, suggesting that both hole and electron trapping are important in the dielectric. The real nature of the charge trapping in the dielectric of capacitive switches is not currently identified.[24]

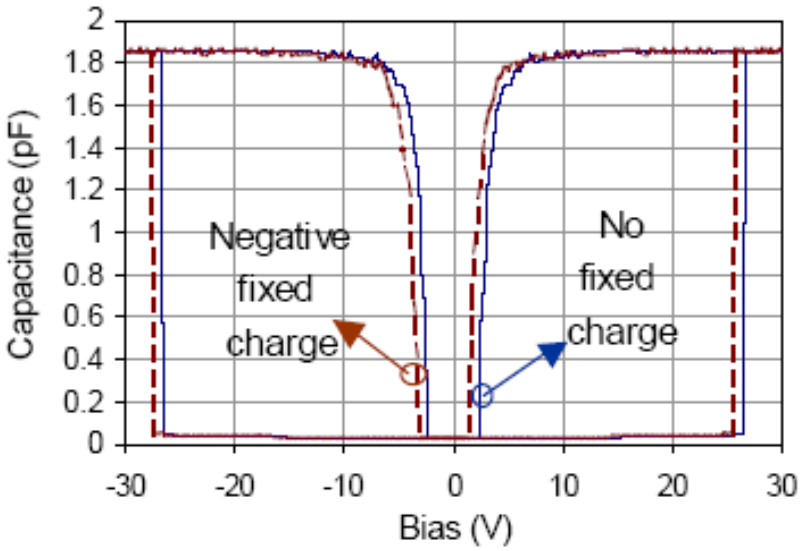

Figure 2.9 The shifts in the C-V curves of the capacitive switch for positive and negative bias that were taken after less than 10^6 cycles (dashed line). Measured C-V curves for one cycle at both biases for the capacitive switch (full line).[25]

Many ideas have been proposed to minimize charge-trapping related failures in capacitive switches. Some researchers have developed different waveforms in order to

reduce the voltage across the dielectric layer. However, these waveforms offer a limited lifetime, and don't eliminate the charge increase in the dielectric.[23] The common waveform taken from PIN diodes circuit is a dual-pulse mode.[26] In this approach, the metal bridge is deflected to the on-state. When the switch is in this state, less holding voltage is required to sustain this position.[23] This decreases the time that the high field is applied across the dielectric and thus the dielectric charging. For example, it has been reported that 5-10 V is sufficient to maintain the switch in an actuated position.[26] As depicted in Figure 2.10 and 2.11, Raytheon has demonstrated lifetimes for capacitive switches up to 10^8 cycles via a dual-pulse mode.[26] As seen in Figure 2.11, it has been demonstrated that when the actuation voltage is dropped from ~60 V to 35 V across the dielectric, the device lifetime improves significantly from 10^4 to 10^8 cycles.[26]

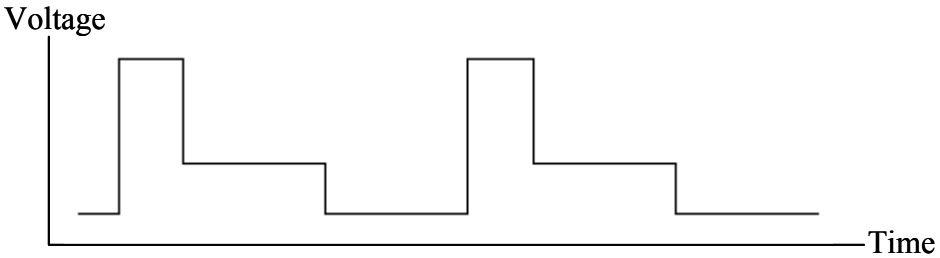

Figure 2.10 Dual-pulse actuation waveform.[26]

Alternatively, another approach to charge-trapping related failures has been to improve the dielectric layer. Many dielectrics have been studied for improving MEMS capacitive switches such as Si_xN_y, SiO_2, Ta_2O_5, $SrTiO_3$, and $Ba_{1-x}Sr_xTiO_3$.[8,16-19] It has been observed that the high-k dielectrics such as $SrTiO_3$ and $Ba_{1-x}Sr_xTiO_3$ have offered high on-off capacitance ratio and low operation voltage.[8,16] Unfortunately, there is no

published information on their lifetimes. Merlijn *et al.*[20] repotted that leaky dielectrics improve the device reliability. This approach was patented by Texas Instruments for the modification of Si_xN_y dielectrics in 1999.[27] In that study, it was proposed to make the silicon nitride leakier so that trapped charges can be easily detrapped.[20,27] Additional information regarding stoichiometry modifications in the silicon nitride is given in the following sections of this chapter.

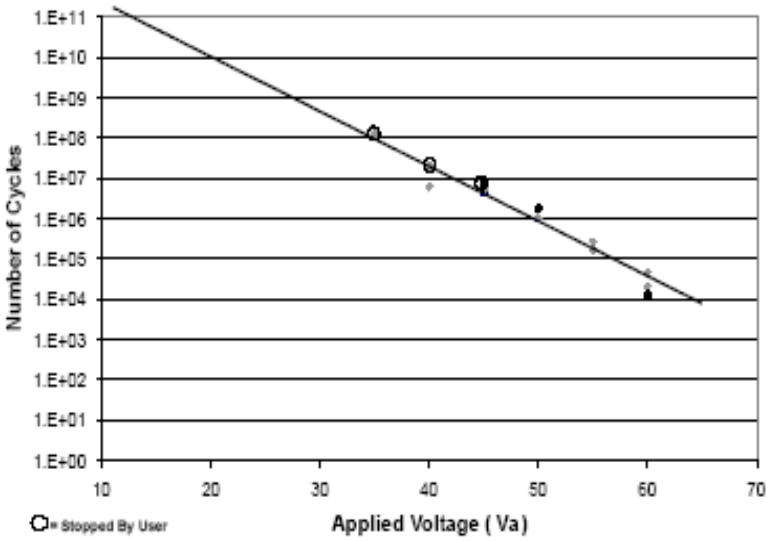

Figure 2.11 Lifetime characterization of the capacitive switch using a dual-pulse waveform at different actuation voltages.[26]

2.5 Structural Properties of Silicon Nitride

Silicon nitride films are widely used in microelectronics as a gate dielectric in thin film transistors, as a charge storage layer in nonvolatile memory devices, and in solar cells.[28] The structural properties of the dielectric have been of great interest to the research community over the years in order to better understand its electrical response in microelectronics.

There are two stable forms of crystalline silicon nitride, the α and β phases.[29] The α phase contains 28 atoms per unit cell and has a space group of $P3_1c$, while the β phase has 14 atoms per unit cell and a space group of $P6_3/m$.[29] The cells differ in the stacking sequence along the z axis.[30] The lattice parameters are a=7.7Å and c=5.6Å for the α phase and a=7.58Å and c=2.9 Å for the β phase.[30] The structural parameters of the α and β phases of Si_3N_4 are summarized in Table 2.2. In both cases, the bonding type is predominantly covalent with some polar character.[31] In addition, the Si atoms are tetrahedrally coordinated by N atoms (sp^3 hybridization) and the N atoms are threefold coordinated by Si in a planar or virtually planar arrangement (sp^2 hybridization).[32]

Table 2.2 Comparison of crystal structure information of α-Si_3N_4 and β-Si_3N_4 with other crystal structures.[30]

Crystal	α-Si_3N_4	β-Si_3N_4	α-SiO_2	Si_2N_2O
Lattice constant (Å)				
a:	7.766	7.586	4.913	8.843
b:				5.437
c:	5.615	2.902	5.405	4.835
Space group	Hexagonal C_{3v}^4	Hexagonal C_{6h}^2	Hexagonal D_3^4	Orthorhombic C_{2v}^{12}
Formula unit *Z*	2	4	3	4
Bond distance (Å)				
Si—N (average)	1.738	1.730		1.714
Si—O (average)			1.610	1.623
Bond angle				
Si—N—Si	118.8	119.9		120
Si—O—Si			144	147.4
Effective charge Q^* in electron				
Si	1.48(0.85)	1.50(0.86)	1.40(0.81)	1.46(0.84)
N	6.89(1.12)	6.87(1.13)		6.90(1.10)
O			7.30(1.02)	7.25(1.01)

Figures 2.12 (a-b) and 2.13 (a-b) show the α and β silicon nitride structures in projection along the [0001] axis and in perspective drawings of the unit cells, respectively. The local structure of amorphous silicon (a-Si_3N_4) as measured by neutron

and x-ray diffraction is reported to be similar to that in crystalline β-silicon nitride.[31]

In ideal a-Si_3N_4, the bonding distance and bond angle are reported to be comparable to crystalline silicon nitride (c-Si_3N_4). In a-Si_3N_4, a uniform Si-N distance of 1.73Å has been measured from neutron scattering and Monte Carlo simulations.[33]

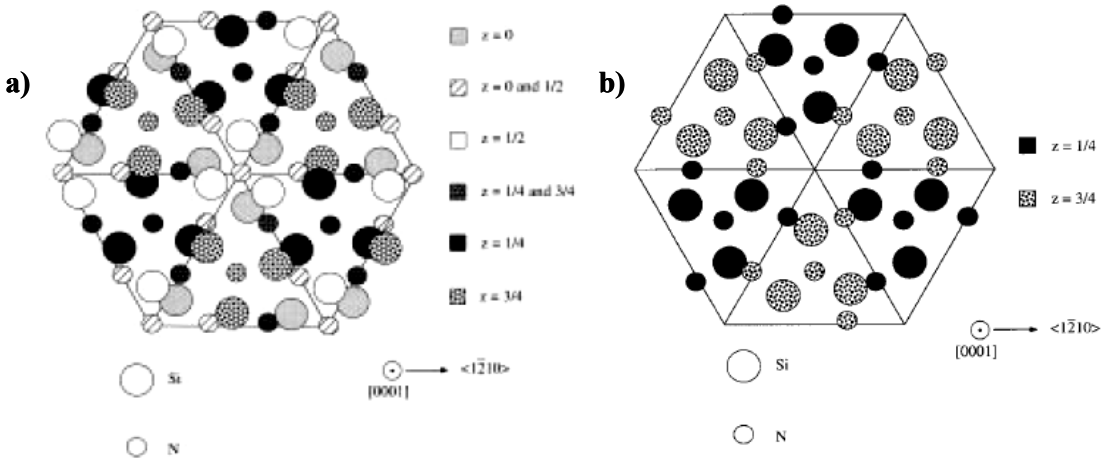

Figure 2.12 a) The α silicon nitride structure in projection along the [0001] axis **b)** The β silicon nitride structure in projection along [0001] axis. Big circles represent silicon atoms and the small ones represent nitrogen atoms.[29]

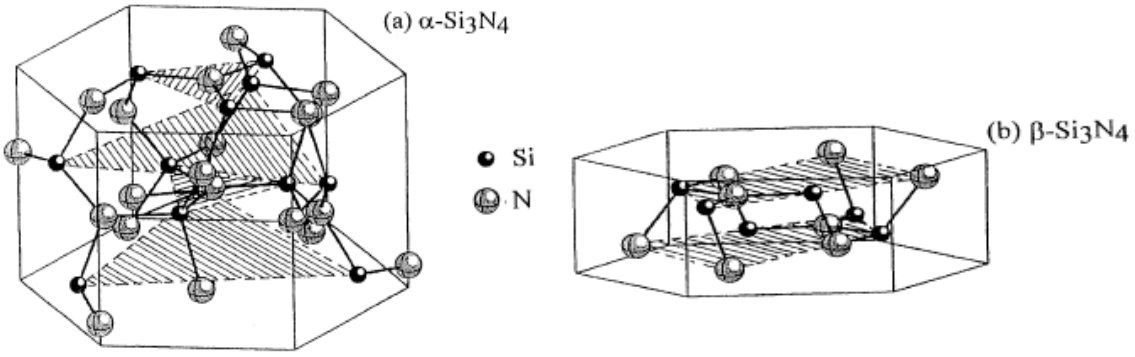

Figure 2.13 Crystal structure of **a)** α-Si_3N_4 **b)** β-Si_3N_4. Shaded planes indicate layer subunits perpendicular to the c-axis.[30]

Additionally, the internal Si-N-Si and N-Si-N angles were measured to be 120° ±4° and 109°±4°, respectively.[33] Silicon nitride films prepared by chemical vapor deposition (CVD) from ammonia (NH_3) and silane (SiH_4) gas mixtures are usually amorphous and contain hydrogen in the range between 10% and 35%.[29] In amorphous silicon nitride, nitrogen has a chemical preference to bind to three silicon atoms, but silicon may bind to other silicon atoms.[34] Hence, dangling bonds may form due to the distorted structure. This phase is generally believed to be an amorphous network consisting of Si-Si, Si-N, Si-H and N-H bonds with bond energies of 1.83 eV, 3.5eV, 3.0eV, and 4.0eV, respectively.[35] The N-N bond is believed not to exist due to its lower energy (1.65eV) compared to the others. Figure 2.14 shows the interaction energy between atoms measured using the Tersoff potential model reported by Mota[33] *et al*.

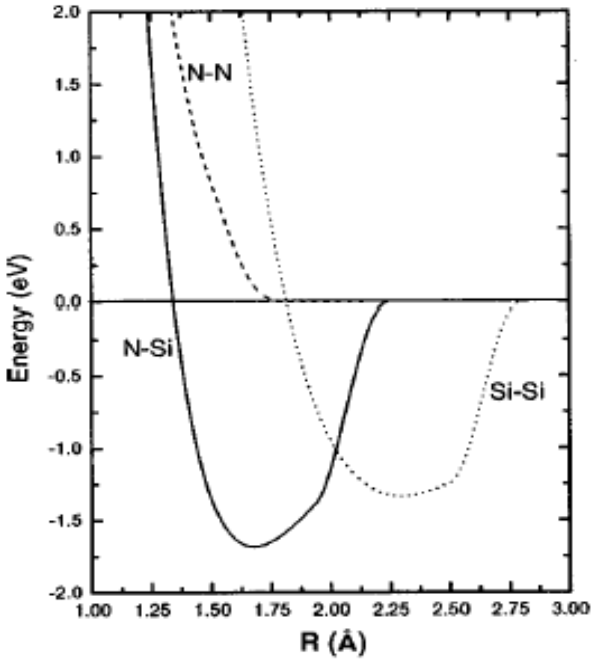

Figure 2.14 The interaction energy of Si-Si (dotted line), Si-N(full line),and N-N (dashed line) bonds.[33]

From Figure 2.14, the Si-N interaction is stronger than the others and provides a shorter equilibrium distance than the Si-Si interaction. The N-N interaction contains the only repulsive term.

2.6. Dangling Bonds in Silicon Nitride

In non-ideal amorphous materials, structural defects can form during deposition. In chemical vapor deposited (CVD) silicon nitride, defects are thought to include N and Si dangling bonds.[32]

Warren *et al.*[36] have reported that nitrogen dangling bonds have been observed in both stoichiometric LPCVD (low pressure chemical vapor deposition) and N-rich PECVD (plasma enhanced chemical vapor deposition) a-SiN_x:H. They reported that paramagnetic defect centers were formed due to the post-deposition annealing (>500^oC) causing hydrogen evolution from N-H site, leaving behind charged N^- ($^-N=Si_2$) and N^+ ($^+N=Si_2$) dangling sites as paramagnetic defect centers in LPCVD and N-rich PECVD a-SiN_x:H.

In their earlier work, they investigated Si and N dangling bonds for different post-deposition annealing temperatures in the a-SiN_x:H using electron paramagnetic resonance (ESR), and reported that N dangling bonds were only observed for x >1.3 and Si dangling bonds were monitored for x<1.3 after anneal/UV procedures.[35] This study is summarized in Table 2.3, showing that the concentration of nitrogen dangling bonds changes with N/Si ratio and annealing temperature in PECVD a- SiN_x:H films.

Table 2.3 The detection of N dangling bonds in PECVD SiN_x:H for different gas ratios ($R=NH_3/SiH_4$), temperatures (T), and compositions (x) measured by ESR.[37]

T_s (°C)	$R=NH_3/SiH_4$	x	Nitrogen dangling bonds
400	3	0.92	No
250	3	0.95	No
250	5	1.20	No
250	7.3	1.35	Yes
500	12	1.49	Yes
400	12	1.55	Yes
250	12	1.61	Yes
250	40	1.63	Yes

2.7 Charge Trapping in Silicon Nitride Dielectric Films

As described above, charge trapping in the silicon nitride dielectric layer is one of the major problems that can affect the reliability of capacitive MEMS switches. When switches are actuated by turning them on and off, the high electric field across the thin dielectric layer causes positive and negative charges to tunnel into the dielectric and become trapped.[23] These charges lead to an applied electric field, causing the metal bridge to stick to the dielectric layer.

The mechanism for charge trapping in silicon nitride is still not well understood. One common idea is that the source for the charge trapping in silicon nitride is silicon or nitrogen dangling bonds.[38] Kirk[32] investigated charge trapping in hydrogenated amorphous silicon nitride (a-SiN_x:H), and proposed that nitrogen dangling bonds are the main trapping sites in MNOS (metal–nitride-oxide-silicon) systems. However, Robertson and Powell[39] reported that silicon dangling bonds caused charge trapping in a-SiN_x:H. Most subsequent reports have supported the idea proposed by Robertson and Powell.

2.7.1 Charge Trapping Due Si Dangling Bonds

Charge tapping due to Si dangling bonds was studied by Robertson and Powell.[39] It has been proposed that dangling bonds form states that can trap either holes or electrons.[38] As shown in Figure 2.15, the silicon and nitrogen dangling bond densities were calculated for CVD deposited Si_3N_4 using the tight-binding and recursion methods.[40] It is proposed that Si dangling bonds form states approximately at 4.2eV, just under the conduction-band minimum (see Figure 2.15-a) and N dangling bonds at -2 eV, near the valence-band maximum (see Figure 2.15-b) in silicon nitride.[40] The band gap was approximately 5.2 eV for the studied films. It has been suggested that N dangling bonds have no contribution to charge trapping due to forming a state out of the band gap (-2eV).

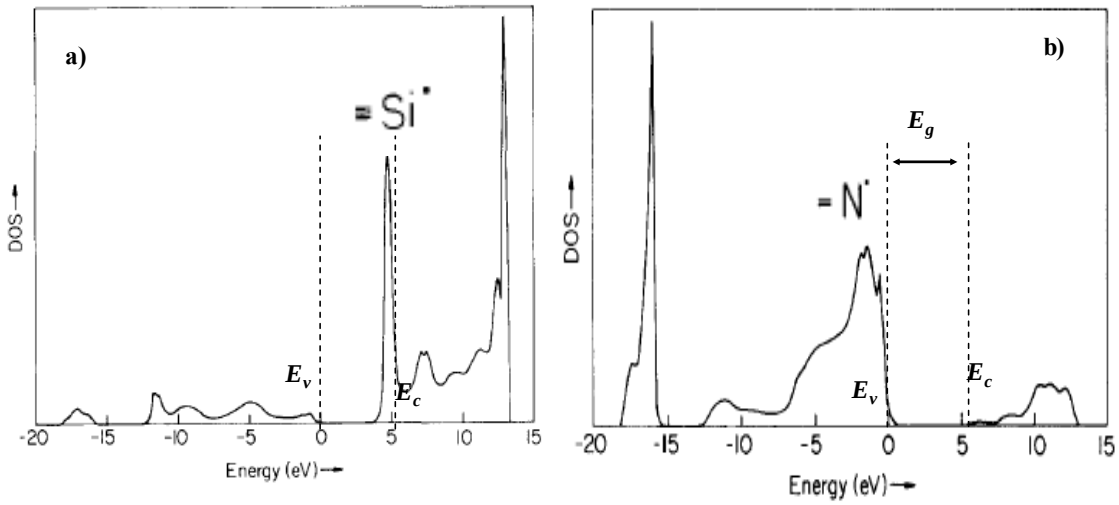

Figure 2.15 The local density of states (DOS) for **a)** Si dangling bond site (≡Si•) **b)** N dangling bond site(=N•). E_v ,E_c, and E_g are valence band energy, conduction band energy, and band gap, respectively.[40]

Charge trapping due to Si dangling bonds was studied by Warren *et al.*[41] using electron paramagnetic resonance (EPR) for PECVD and LPCVD a-SiN_x. In this study,

electrons and holes were injected into the films using a corona discharge apparatus for investigation of charge trapping in the a-SiN_x. It was concluded that Si dangling bonds, *K* centers, were the charge trapping centers in both N-rich and stoichiometric silicon nitride. Neutral centers K^o, ($\bullet Si{\equiv}N_3$) are paramagnetic with an unpaired electron on a silicon atom. However, positively K^+, ($^+Si{\equiv}N_3$) and negatively K^-, ($Si{\equiv}N_3$) charged centers are diamagnetic without unpaired electrons. As electrons are injected into either stoichiometric LPCVD or N-rich PECVD silicon nitride, they can be captured by K^o centers and become trapped there, therefore explaining the observed increase in negative charges. This result suggests that the following reaction occurs during electron trapping at electron paramagnetic resonance -K° centers.[41]

$$K^o + e^- \rightarrow K^- \qquad (2.6)$$

Similarly, when holes are injected into UV-illuminated N-rich PECVD a- SiN_x:H films, the concentration of positive charges increases in the film. This result suggests the following reaction occurring at hole traps at electron paramagnetic resonance -K° centers.[41]

$$K^o + h^\bullet \rightarrow K^+ \qquad (2.7)$$

2.7.2 Charge Trapping Due to N Dangling Bonds

Kirk[32] has proposed that certain point defects due to nitrogen dangling bonds in amorphous silicon nitride, named valence alternation pairs (VAP), are responsible for charge trapping in amorphous silicon nitride. In silicon nitride, nitrogen is normally coordinated by three silicon atoms in a near planar trigonal configuration. The VAP model considers electron traps as defects (represented by N_4) where nitrogen is

coordinated by four silicon atoms and hole traps as defects (represented by N_2) where nitrogen is coordinated by two silicon atoms. The N_4 and N_2 defects can each exist in three different charge states N_4^+, N_4^o, N_4^- and N_2^+ N_2^o, N_2^- , respectively.[32] These charge states occur when electrons and holes occupy the N_4 and N_2 defect centers. An energy–band diagram of N_4 and N_2 defects is given for trap levels in Figure 2.16. The N_4 trap levels were assumed to lie near the conduction bond edge (within 1-2eV) and N_2 trap levels were assumed to lie near the valence band edge (within 1-2eV) in the band gap.[32] N_4 and N_2 trap levels were believed to act as electron and hole traps, respectively. In Figure 2.16, the letters E, W, and U are empty polaron levels, the lattice relaxation energy of defect centers, and Coulumbic repulsion energies of trap centers, respectively. N_4^+ and N_2^- exhibit the lowest energy VAP defect arrangement.

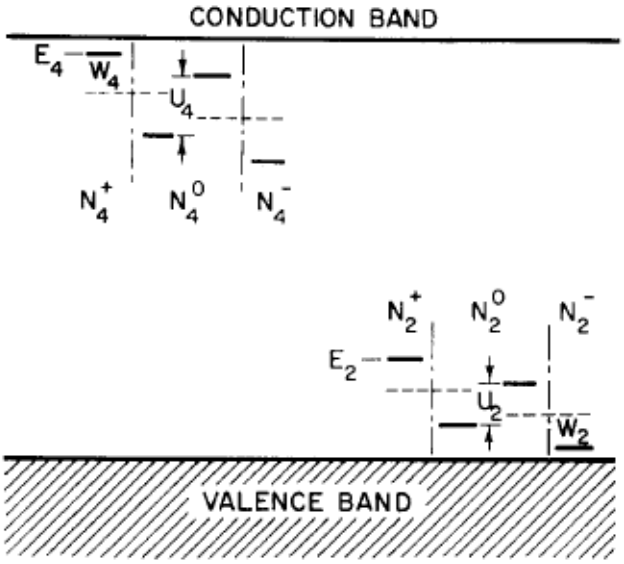

Figure 2.16 Band diagram of a-Si_3N_4 showing the relative positions of the charge capture and emission levels of the proposed N_4 and N_2 VAP defect centers.[32]

The reactions between conduction band electrons and the N_4 defect states are given by[26]

$$N_4^+ + e^- \Leftrightarrow N_4^o \qquad (2.8)$$

and

$$N_4^o + e^- \Leftrightarrow N_4^- \qquad (2.9)$$

The reactions between valence-band holes and the N_2 defect states are given by

$$N_2^- + h^\bullet \Leftrightarrow N_2^o \qquad (2.10)$$

and

$$N_2^o + h^\bullet \Leftrightarrow N_2^+ \qquad (2.11)$$

2.8 The Effect of Si and H Concentration on Charge Trapping

Since the dangling bond formation in silicon nitride is due to defects that can alter the electrical properties, it is also important to mention how the Si content can affect the dangling bond densities involved in the charge trapping.

Bailey *et al.*[42] proposed that when the silicon concentration increases relative to stoichiometric silicon nitride (to Si/N=0.75), the trapped electron density increased approximately twice as measured by Auger electron spectroscopy on MNOS (Metal-Nitride-Oxide-Silicon) samples. Figure 2.17 shows the trapped electron density as a function of the silicon content in the silicon nitride. The excess silicon was introduced into the film during the deposition process. They have proposed that their results were consistent with the valence alternation pair defect model, proposed by Kirk[32] described earlier in this chapter. In this model, the electron traps are caused by defects where nitrogen is bonded to four silicon atoms (named N_4).

The silicon nitride deposited by LPCVD and PECVD contain hydrogen that affects the electrical properties. Hence, hydrogen is another factor that may affect charge trapping states via forming or removing dangling bonds in the silicon nitride. There is a large amount of hydrogen present during deposition of silicon nitride films by CVD approaches due to the use of NH_3 (ammonia) and SiH_4 (silane) gases. Incorporated hydrogen concentrations of 5% to 10% are common for LPCVD and 20% to 30% for PECVD nitride films.[43]

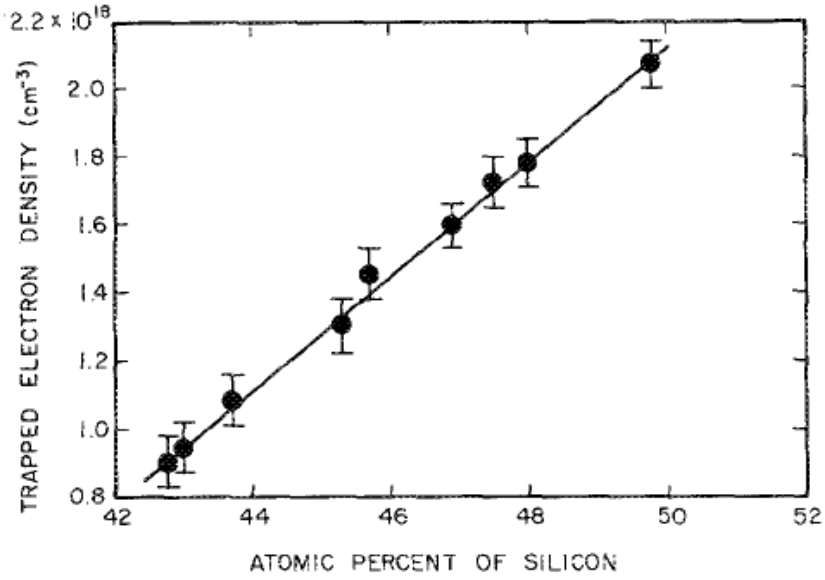

Figure 2.17 The trapped electron density as a function of the silicon content in the Si_xN_y measured by Auger electron spectroscopy.[42]

Mota *et al.*[44] proposed that hydrogen bonds to silicon and nitrogen in the amorphous silicon nitride, significantly decreasing the number of dangling bonds. They studied $SiN_{1.33}:H_y$ for different hydrogen contents ($0\%<y<40\%$). Figure 2.18 shows the percentage of under-coordinated Si and N atoms as a function of the hydrogen content. As depicted, the concentrations of under-coordinated silicon and nitrogen atoms decrease

with increases in the hydrogen content. In addition, the nitrogen dangling bond concentration decreases faster than the silicon dangling bond concentration.

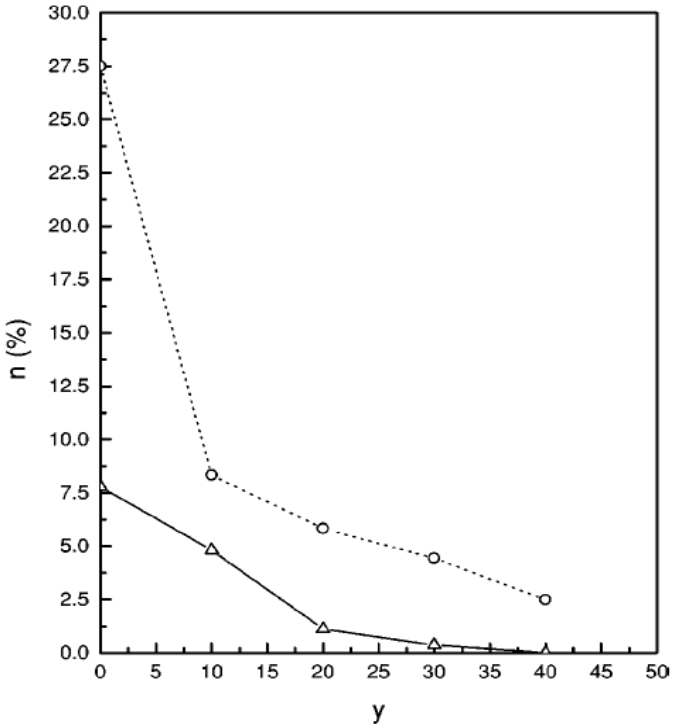

Figure 2.18 Concentration of under-coordinated Si (triangular) and N (circle) as a function of hydrogen content, y (in at.%).[44]

In contrast, Kapoor *et al.*[43] studied amorphous stoichiometric silicon nitride (a-Si_3N_4) films deposited by PECVD in MNOS systems and proposed that the trapped electron density increased with hydrogen content in the silicon nitride. They measured the hydrogen concentration as function of the trapped electron density using a photoelectric effect technique in a combination with nuclear reaction analysis. As shown in Figure 2.19, for an increase in the hydrogen concentration of around 3 at. %, the trapped electron density increased by a factor of approximately 3.5 from $0.55x10^{18}$ to $2x10^{18}$ cm^3. Robertson[40] developed a possible explanation for this behavior. He reported

that hydrogen is not active for removing dangling bond states in silicon nitride, and thus it saturates Si dangling bond states that lie in the band gap. However, he observed that hydrogen is an effective passivant of nitrogen dangling bonds (silicon nitride with N dangling bonds) due to forming a state out of the band gap.

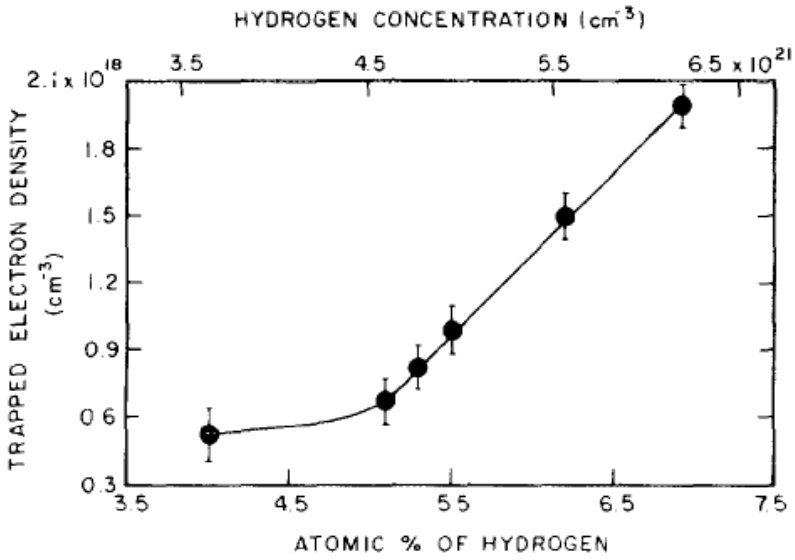

Figure 2.19 Trapped electron density as a function of hydrogen concentration in Si_3N_4 measured by nuclear reaction analysis.[43]

2.9 Electronic Properties of Non-Stoichiometric Silicon Nitride

The electronic properties of silicon nitride films change with the silicon/nitrogen ratio. It has been observed by many researchers that nitrogen rich silicon nitride has a larger band gap than silicon rich compositions. Figure 2.20 (a) shows x values determined by XPS as a function of the deposition gas ratios in SiN_x:H films deposited at 300°C using a PECVD process.[45] It can be seen that the x values of the SiN_x:H increase as the ammonia/silane ratios (R) are increased from 0.2 to 5. Figure 2.20 (b) shows the

optical band gap of the same films as a function of the ammonia/silane ratios (determined by fitting the data to a Tauc plot of absorption coefficients) [46]

$$\alpha h\nu = C_2(h\nu - E_o)^2 \qquad (2.12)$$

where α is the absorption coefficient, $h\nu$ is the photon energy, C_2 is a constant, and E_o is the optical band-gap energy. It can be seen that the band gap increases sharply for R>1.

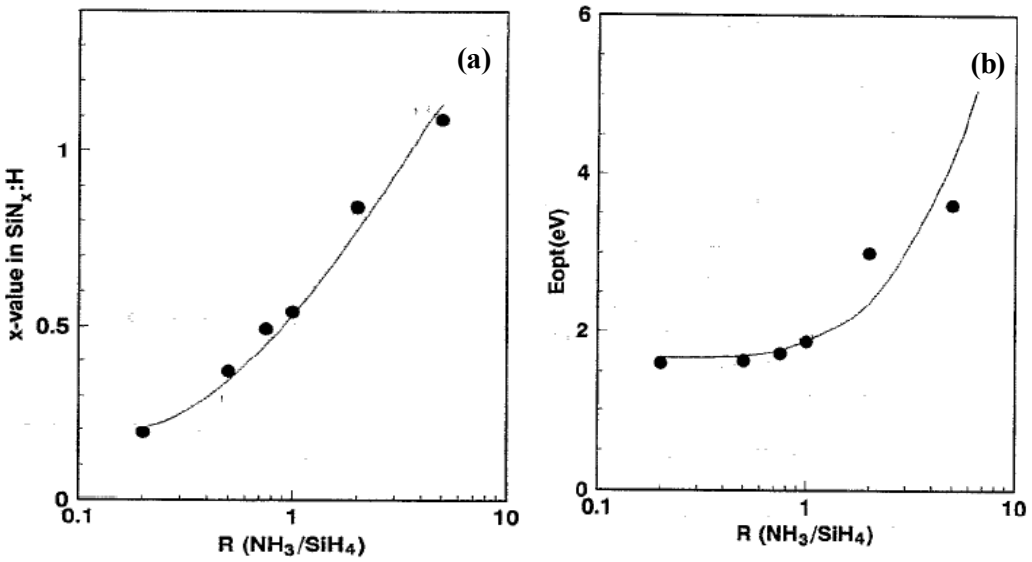

Figure 2.20 a) x values of SiN_x:H films measured by XPS as a function of the gas ratio (R). **b)** Optical band gaps E_{opt} obtained from Tauc plots as a function of the gas ratio.[45]

Additionally, as depicted in Table 2.4, the optical band gap changes with x values in Si- rich SiN_x:H films deposited by the glow-discharge technique at 300°C.[46] As seen there, the optical band gap (E_o) increases from 1.66 to 2.34, as x is increased from 0 to 0.84.

Furthermore, the bonding configurations in the silicon nitride generate different defect states (N-dangling or Si-dangling) in the optical band gap and thus these arrangements affect the conductivity of the silicon nitride. Masaki *et al.*[45] proposed a

Table 2.4 Optical band gap for various SiN_x:H compositions. E_{04} values are where α is $10^4 cm^{-1}$.[46]

R	x	E_0 (eV)	E_{04} (eV)	$c_2/10^5$ ($cm^{-1} eV^{-1}$)
0	0	1.66	1.88	4.00
1	0.32	1.83	2.08	3.60
2	0.69	2.07	2.38	2.6
4	0.95	2.24	2.65	1.9
6	0.84	2.34	2.73	1.8

schematic band diagram for PECVD SiN_x:H, demonstrating the calculated variation of the band gap with the gas ratio R (NH_3/SiH_4). As depicted in Figure 2.21(a), as the nitrogen content increases (the gas ratio R>1), the optical band gap (E_o) of the SiN_x: H increases and the slope of the band edge decreases. Si-rich silicon nitride possesses a lower band gap than N-rich silicon nitride. Warren *et al.*[37] proposed a similar form for the

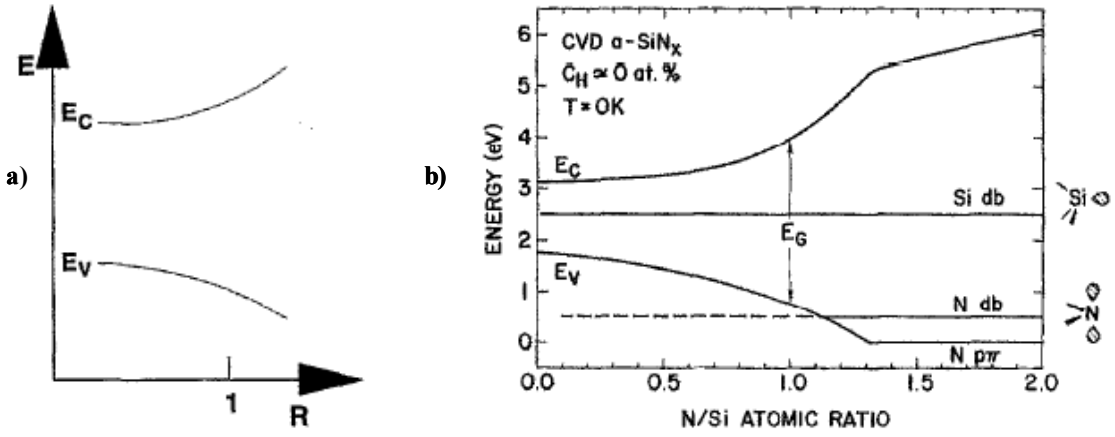

Figure 2.21 Schematic band diagrams **a)** for SiN_x:H films as a function of gas ratio R proposed by Masaki *et al.*[45] The tail states extend further into the band gap with increasing R for R<1 **b)** for a-SiN_x as proposed by Warren *et al.*[37] Band edges and defect energy states are shown as a function of N/Si ratio. E_c, E_v, and E_G are the conduction band energy, valence band energy, and band gap of the silicon nitride, respectively. Si_{db} and N_{db} are silicon dangling bonds and nitrogen dangling bonds.

change in band gap as a function of N/Si ratio using the tight binding method for a-SiN_x deposited by PECVD. Additionally, as shown in Figure 2.21 (b), they speculated that Si dangling bonds lie in the midgap for all compositions and that N dangling bonds yielded energy states above the valence band (E_v) edge for N-rich compositions (N/Si>1.3).

The optical gap band, composition, and refractive index can be related to each other in silicon nitride. Figure 2.22 shows the optical band gap of the a-SiN_x:H deposited by PECVD technique extracted from Tauc plots as a function of gas ratios for different RF power densities.[38] As seen in the figure, as the Si content is increased, the gap decreases and the refractive index increases. The bonding environment of the N-H, Si-H,

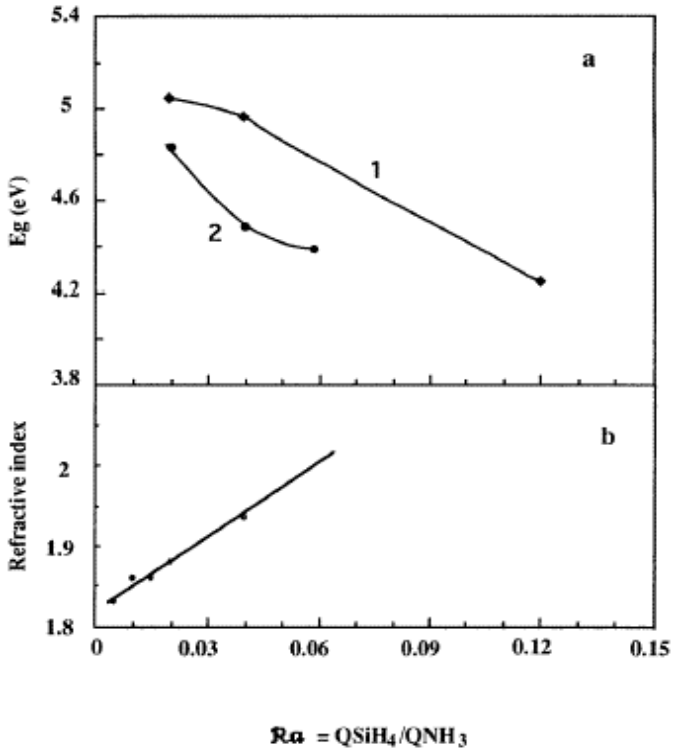

Figure 2.22 (a) The optical band gap of the a-SiN_x:H extracted from Tauc plots as a function of gas ratios for different RF power densities 37 (2) and 53 $mW.cm^{-2}$ (1) **(b)** The refractive index as a function of gas ratios (Ra).[38]

and Si-N significantly depends on the N/Si (gas ratio) and deposition technique. Modification in the bonding density affects the refractive index of silicon nitride. It was reported that the refractive index of PECVD silicon nitride and the bond density of Si-H and N-H varies with the silane flow ratio.[47] Table 2.5 shows the effect of silane flow rates on the properties of PECVD silicon nitride. The films were deposited at 250°C and 350°C for silane flow rates from 5 sccm to 30 sccm (standard cubic centimeters per minute). As seen in Table 2.5, for a low silane flow rate (<15sccm), the silicon nitride is nitrogen-rich (N/Si>1.33) with low refractive indexes, but films made with a flow rate higher than 17sccm were silicon rich with higher refractive indexes. The lowest hydrogen density was obtained for the stoichiometric composition with a N/Si ratio of 1.33 measured by RBS (Rutherford backscattering).

Table 2.5 Effect of silane flow rate on properties of PECVD silicon nitride films.[47]

Sample number	Run ID number	Flow rates $SiH_4/N_2/He$	Substrate temp(C°)	Thickness (Å)	Dep rate (Å/min.)	Etch rate (Å/min.)	Refractive index	N/Si ratio	Si-H ($\times 10^{21}$ cm^{-3})	N-H
1	730	5/500/1300	250	620	12	399	1.830		···	15
2	904-2	10/500/1300	250	830	28	231	1.854	1.50	0.8	13
3	1204	14/500/1300	250	950	43	68	1.923	1.39	3.1	6.0
4	1205	15/500/1300	250	980	44	70	1.928	1.36	3.6	4.8
5	108	16/500/1300	250	1050	48	72	1.967	1.31	6.4	4.0
6	920-2	17/500/1300	250	1020	51	85	1.985	1.23	7.9	2.4
7	904	20/500/1300	250	900	53	66	2.06	1.12	8.7	1.6
8	604	30/500/1300	250	1090	64	44	2.44	1.00	16	···
9	109	15/500/1300	350	920	42	17	1.987	1.31	3.4	2.3

In addition, Figure 2.23 shows the N-H and Si-H bond concentrations as a function of silane flow ratio.[47]As seen, the N-H bond concentration decreases with an increase in the silane flow, while the Si-H bond concentration increases with silane flow ratio.

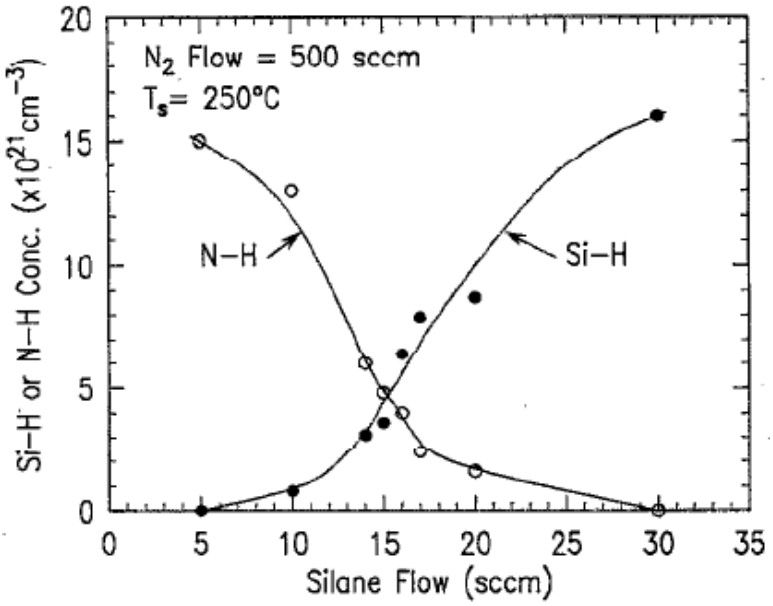

Figure 2.23 Si-H and N-H bond concentration as a function of the silane flow rate.[47]

2.10 Electrical Conduction in Thin Dielectric Films

Carrier transport in the insulator of an MIM capacitor under an electric field not only depends on the insulator itself but also on the interaction of the insulator with its electrodes.[48] Consequently, conduction can be classified as either bulk-limited (Poole-Frenkel, Ohmic, and Space-Charge-Limited) or electrode-limited (Schottky and Fowler-Nordheim).[49]

In terms of electrode limited conduction, charge injection into the insulator from the metal occurs over interfacial Schottky barriers which can be modified by the work function of the electrode.[48-49] Charge injection at an interface might arise at very high fields through a triangular barrier from the metal Fermi level into the conduction band of the insulator via Fowler-Nordheim tunneling.[48] In addition, the injection can occur without an interfacial barrier limitation by means of Ohmic conduction.[49] Conversely, in

the bulk of the insulator, the conduction can be dominated by the Poole-Frenkel effect due to trapping and detrapping of carriers.[50] Figure 2.24 illustrates charge injection and conduction in the insulator due to the applied electric field in an MIM capacitor.

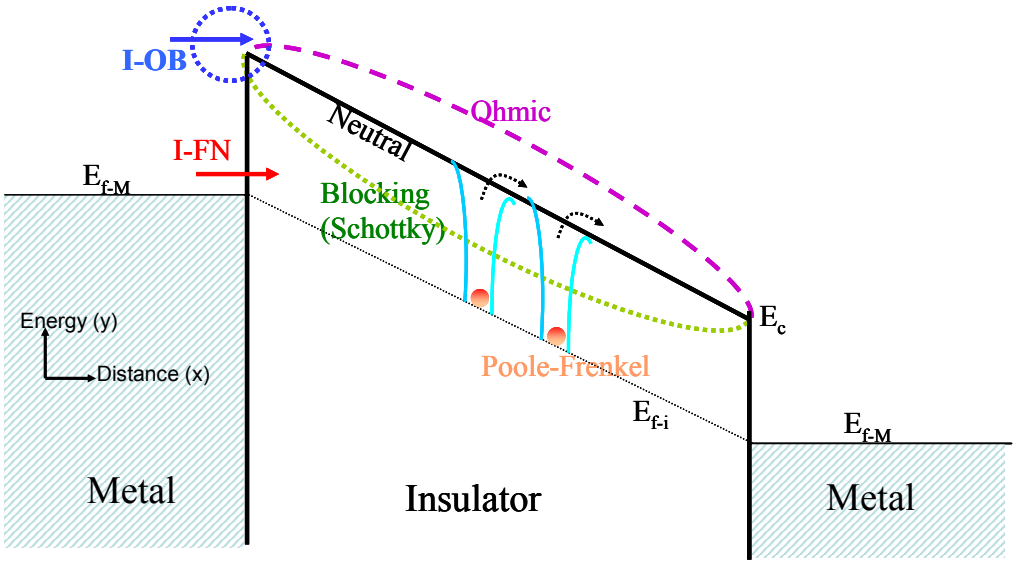

Figure 2.24 Schematic of charge injection and conduction in an MIM structure under an electric field. $E_{f\text{-}m}$, and $E_{f\text{-}i}$ are Fermi energy of metal and insulator. E_c is the conduction band energy of the insulator. I-OB and I-FN signify charge injection over a barrier and injection due to Fowler-Nordheim tunneling.[49,51]

2.10.1 Poole-Frenkel Effect

The Poole-Frenkel effect can be defined as the thermal emission of charge carriers from Coulombic trap levels into the conduction or valence band of an insulator due to the applied electric field.[49] The electric field lowers the barrier height on one side of the trap potential well, thus increasing the probability of the electron escaping from the trap.[52] Figure 2.25(a-b) illustrates the field-induced barrier lowering.[52] In order for Poole-Frenkel emission to occur, the trap is required to be neutral when filled with an electron and positively charged when the electron is emitted.[50] Thereby, the attraction between the

positively charged trap and the electron provides a Coulombic force, named a Coulombic attractive center.[49]

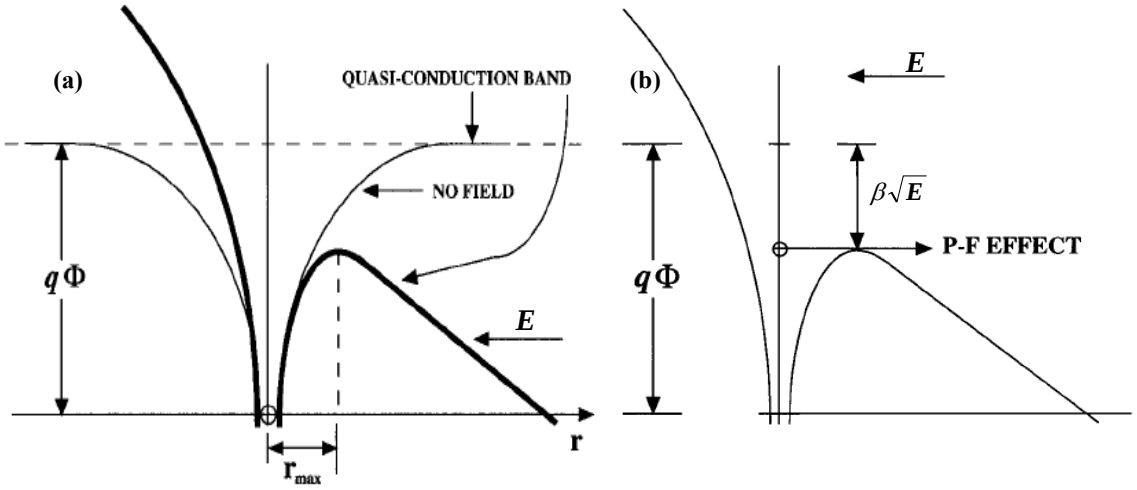

Figure 2.25 a) Coulombic potential well. The thin lines show the potential with no field applied, and thick lines represent the effect of an electric field **b)** The Poole-Frenkel effect of the Coulombic potential well under an electric field.[52]

In Figure 2.25(b), $q\Phi$ is the amount of energy needed for the electron to escape from the trap without an electric field and $\beta.E^{1/2}$ is the amount by which the trap barrier height is reduced by the applied electric field (E). The reduction in the trap barrier height due to the electric field is given by[52]

$$\Delta q\Phi = \beta\sqrt{E} \qquad (2.13)$$

where β is the Poole-Frenkel field lowering coefficient defined by

$$\beta = \sqrt{\frac{q^3}{\pi\varepsilon_o\varepsilon_r}} \qquad (2.14)$$

In this equation q, ε_o, and ε_r are the electronic charge, the permittivity of free space, and the high-frequency dielectric constant of the insulator, respectively. When an electric

field is applied to the system, the effective trap barrier height is $q\Phi–\beta.E^{1/2}$. Consequently, due to the barrier reduction, the electrical conductivity (σ) as a function of electric field can be written as[49]

$$\sigma = \sigma_o \exp(\frac{\beta\sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \qquad (2.15)$$

where σ_o is the conductivity at zero electric field given by

$$\sigma_o = \boldsymbol{C} \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \qquad (2.16)$$

where *C, k,* and *T* are a proportionality constant, Boltzmann's constant, and the absolute temperature, respectively. Equations 2.15 and 2.16 describe the field and temperature dependence characteristic of the Poole-Frenkel effect. The current density (J) due to the Poole-Frenkel effect is obtained by multiplying the conductivity given in Equation 2.15 by the electric field, yielding[52]

$$\boldsymbol{J} = \boldsymbol{E} \times \sigma = \boldsymbol{E} \times \boldsymbol{C} \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \exp(\frac{\beta\sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \qquad (2.17)$$

However, in order to experimentally confirm that Poole-Frenkel dominates the conduction, the data fitted to Equation 2.17 at high fields must provide a dynamic relative dielectric constant for the insulator material that is close to the value measured separately at optical frequencies.

2.10.2 Schottky-Richardson Emission of Carriers at Metal-Insulator Interface

When the conduction of carriers is limited by a metal-insulator interfacial potential barrier which doesn't permit tunneling to occur, the current flowing through the insulator is controlled by the probability of carriers being thermally emitted over the

barrier into the insulator conduction band.[53] Accordingly, the temperature dependence of the thermoionic emitted current is described by[49]

$$\boldsymbol{J} = \boldsymbol{A} \times \boldsymbol{T}^2 \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \tag{2.18}$$

where A is the effective Richardson constant, which incorporates the carrier mobility, Φ is the interfacial barrier height, q is the carrier charge, T is temperature, and k is Boltzmann's constant. The injection of carriers is assisted by image forces due to electrons polarizing the surface of the metal from which they are injected; thereby the interfacial barrier (Φ) varies with applied electric fields. Figure 2.26 illustrates this effect. The reduction of interfacial barrier height due to the electric field, E thus given by [49]

$$\Delta \boldsymbol{q}\Phi = \beta\sqrt{\boldsymbol{E}} \tag{2.19}$$

β is the field lowering coefficient defined by

$$\beta = \sqrt{\frac{\boldsymbol{q}^3}{4\pi\varepsilon_o\varepsilon_r}} \tag{2.20}$$

In this equation q, ε_o, and ε_r are the electronic charge, the permittivity of free space, and the high-frequency dielectric constant of the insulator, respectively. In order to obtain the current density due to the Schottky-Richardson effect, the barrier height in Equation 2.18 should be replaced by the effective barrier, qΦ-qΔΦ.[53]

Equation 2.17 can be rewritten by [49,53]

$$\boldsymbol{J} = \boldsymbol{A} \times \boldsymbol{T}^2 \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \exp(\frac{\beta\sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \tag{2.21}$$

To confirm that the conduction through the insulator is controlled by this effect, the current density-electric field data fitted to this equation should provide a dynamic

dielectric constant (from the slope of linear part) that agrees with the measured high frequency value.[50]

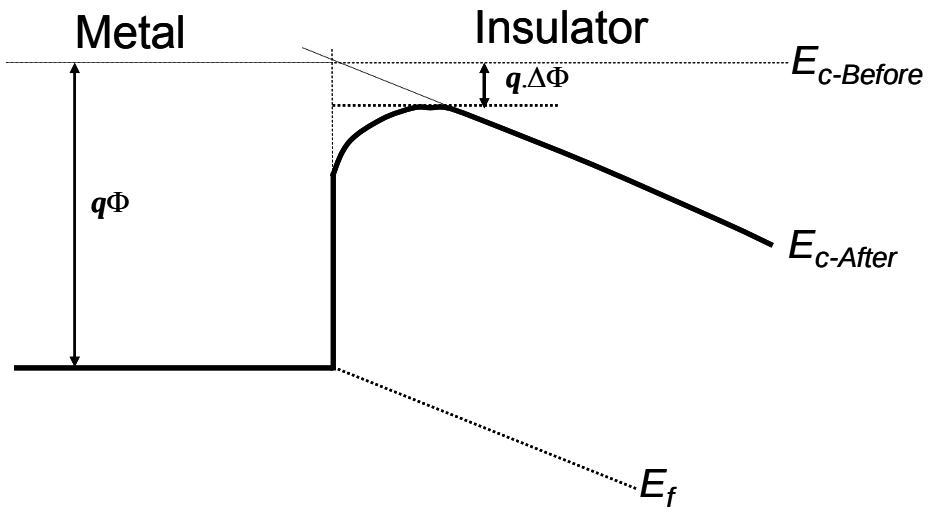

Figure 2.26 Schematic of thermoionic emission of electrons from a metal into an insulator due to the lowered barrier at the interface with the electric field. $E_{c\text{-}Before}$ and $E_{c\text{-}After}$ are conduction band shapes before (dashed line) and after (full line) the application of electric field.[49]

2.10.3 Fowler-Nordheim Tunneling

The injection of carriers from a metal into the insulator may occur without thermal emission of carriers over the interfacial potential barrier when a sufficiently strong electric field is applied.[48] In this case, the potential barrier at the interface may become very thin (usually <10nm), enabling carriers to tunnel into the insulator conduction band from the metal Fermi level.[53] Tunneling depends on the applied electric field (**E**) and insulator thickness ($\mathbf{d_i}$). Fowler-Nordheim tunneling may occur when the interfacial potential barrier ($\mathbf{\Phi_B}$) satisfies the following relation[55]

$$\boldsymbol{E x d_i} \geq \Phi_B \qquad (2.22)$$

Figure 2.27 illustrates a schematic of this phenomenon.

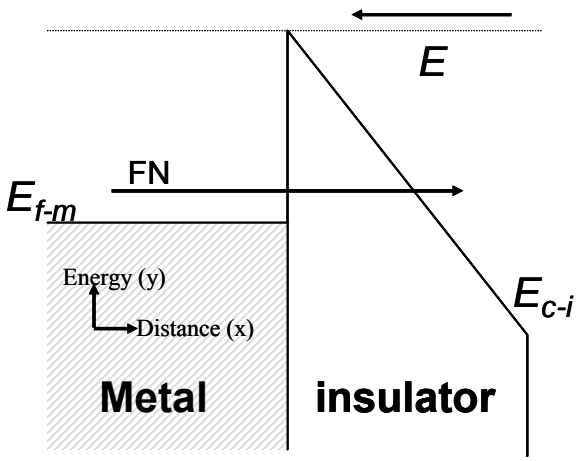

Figure 2.27 Fowler-Nordheim tunneling through a triangular barrier at a Metal-Insulator interface. Arrows indicates the Fowler-Nordheim injection level through a triangular potential barrier and E is applied electric field direction. $E_{f\text{-}m}$ and $E_{c\text{-}i}$ are a metal Fermi energy level and insulator conduction band energy.[49]

Fowler-Nordheim tunneling is independent of temperature[54], and yields a current density as follows[55]

$$J_{FN} = \frac{q^2 E^2}{16\pi^2 \frac{m^*}{m} \hbar \Phi_B} \exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E} \right] \tag{2.23}$$

where m is the mass of an electron in free space, m^* is the effective mass of an electron in the crystal ($m \approx 0.4m^*$), $\hbar$ is Planck's constant/2π, and Φ_B is the barrier height for tunneling.

2.10.4 Ohmic Conduction

Ohmic conduction is limited by the thermal activation of carriers into the conduction band of the insulator, rather than by the metal-insulator barrier.[49] When the

interface barrier is small enough to permit a sufficient charge carrier emission, the contact metal has no influence on the current flow.[49] Hence, the bulk controlled current density increases linearly with applied electric field according to Ohm's law. The current density ($\boldsymbol{J}$) due to Ohmic conduction is given by[56]

$$\boldsymbol{J} = \sigma_o \boldsymbol{E} \exp(\frac{\boldsymbol{E}_A}{\boldsymbol{kT}}) \qquad (2.24)$$

where σ_o, E_A, and E are a pre-exponential parameter, the thermal activation energy and the electric field, respectively.

2.10.5 Space-Charge Limited Conduction (SCLC)

Space-charge-limited conduction occurs when charge injection into the conduction band of an insulator isn't limited by a metal-insulator barrier; the injected charges form a space charge layer that limits current flow.[49] Hence, the space-charge effect is bulk limited.[49] The current-voltage relation shows Ohmic behavior at low voltages where the emission from electrodes is much lower than the rate of thermoionic generated charge carriers in the bulk.[57] The current density-voltage (J-V) relation of these Ohmic regions is given by[57]

$$\boldsymbol{J} = \boldsymbol{q}\boldsymbol{n}_o \mu(\frac{\boldsymbol{V}}{\boldsymbol{d}}) \qquad (2.25)$$

where q, n_o, $\mu_{,,}$ and d are the electronic charge, concentration of charge carriers, mobility of carriers, and film thickness, respectively. Conversely, the space-charge current-voltage response occurs at higher voltages and depends on the trap density in the film.[49] In this case, the current density-voltage relation in materials with shallow traps is given by[57]

$$J = \frac{9\theta\mu\varepsilon_r\varepsilon_o V^2}{8d^3} \qquad (2.26)$$

where Θ is the ratio of the free carrier density and the density of the filled trapping sites (Θ =1 for a defect-free material). μ, ε_r, ε_o and d are the mobility of carriers, dielectric constant of the film, permittivity of free space and film thickness, respectively.

2.11 Electrical Conduction in Silicon Nitride Dielectric Films

Electrical conduction in silicon nitride dielectrics has been studied by many researchers. In this dielectric, the conduction mechanism was observed to be Poole-Frenkel at high fields. Fowler-Nordheim tunneling was only suggested to occur for very thin films at high fields. However, Ohmic conduction has been proposed for low fields. The following paragraphs summarize the studies with the likely conduction mechanisms in silicon nitride dielectrics for all field levels.

The current-voltage (I-V) relation of silicon nitride dielectric films is strongly dependent on stoichiometry. It has been observed by many researchers that when silicon nitride is prepared increasingly silicon rich, the current density increased significantly. Kato *et al.*[54] studied current conduction in silicon nitride and silicon oxynitride with different compositions deposited at 400 ^{o}C by PECVD. They observed that the current density of silicon nitride films increased when the N/Si ratios were decreased from 1.26 to 0.9. Figure 2.28 shows the current density as a function of the electric field for different compositions in silicon nitride and oxynitride films. It can be seen that the current density of Si-rich silicon nitride (curve D) reaches approximately 10^{-3}A.cm^{-2} at an electric field of 4MV.cm^{-1} while for the composition containing more nitrogen (curve F),

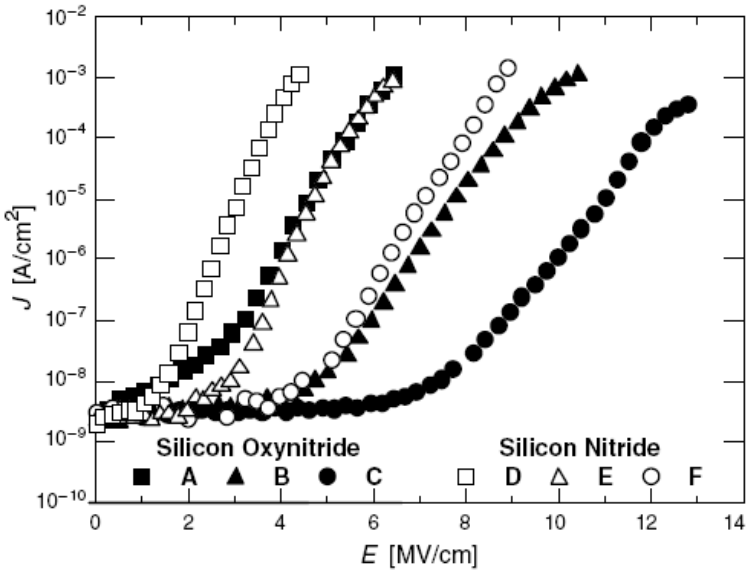

Figure 2.28 The current density as a function of the electric field in the silicon nitride and silicon oxynitride measured at room temperature (25 °C).[54]

8MV/cm is required to reach the same current density. Additionally, silicon oxynitride and silicon nitride reveals similar current densities as a function of the electric field.

The Poole-Frenkel effect has been observed by other researchers for Si-rich and stoichiometric silicon nitride at high fields. The ability to observe this effect at room temperature in silicon nitride dielectrics completely depends on the applied field and stoichiometry. It has been commonly seen that the Poole-Frenkel effect could be observed at lower electric fields for Si-rich compositions compared to N-rich compositions.[47] As depicted in Figure 2.29, for films that were deposited at 400°C by a PECVD process, the Poole-Frenkel effect is observed approximately above 1MV.cm^{-1} for Si-rich silicon nitride (F on Figure) with N/Si of 0.9 and above 4MV.cm^{-1} for the composition (D on Figure) with a N/Si ratio of 1.26 (see linear fitted the part of curves on the graph).[58] Kaya *et al.*[59] studied Poole-Frenkel conduction of Si- rich PECVD silicon

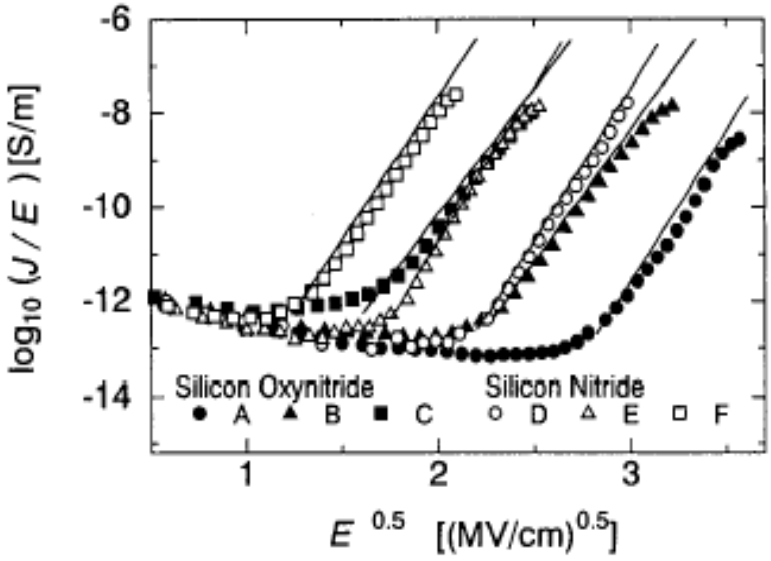

Figure 2.29 Poole-Frenkel plots for a-SiN_z:H and a-SiO_xN_y:H measured at 25 °C. Films were deposited at 400 °C by PECVD process.[58]

nitride films deposited at 250°C with flow rate ratios ($R=NH_3/SiH_4$) between 0.5 and 0.8 (Si-rich). They calculated a dynamic dielectric constant between 3 and 4 from the slope of the Poole-Frenkel fit to the data. In addition, Hsieh *et al.*[60] reported dynamic relative dielectric constants between 3.52 and 4.10, obtained from Poole-Frenkel slopes for the Si-rich PECVD a-SiN_x:H deposited at 300 °C. However, Parsons *et al.*[47] estimated a dielectric constant of 4.37 for stoichiometric PECVD silicon nitride (N/Si=1.33) deposited at 250 °C. They compared this value with its refractive index of 1.98 (λ=6328 Å) measured by ellipsometry. As a result, all researchers [47,58-60] agree that the Poole-Frenkel mechanism dominates conduction in silicon nitride films at high fields with dynamic dielectric constants in the range between 3 and 4.4.

Furthermore, the trap barrier heights can be deduced from the Poole-Frenkel active regions. Figure 2.30(a) shows Poole-Frenkel active regions (the linear part of the

curve where it provides a dynamic dielectric constant of ~3.1) at room temperature at fields above approximately 1 MV.cm^{-1} for Si-rich silicon nitride deposited at a gas flow ratio of 0.75 (R=NH_3/SiH_4) by a PECVD process at 300^{o}C.[45] For the same active regions, Figure 2.30 (b) shows conductivities as a function of temperature at constant voltages.

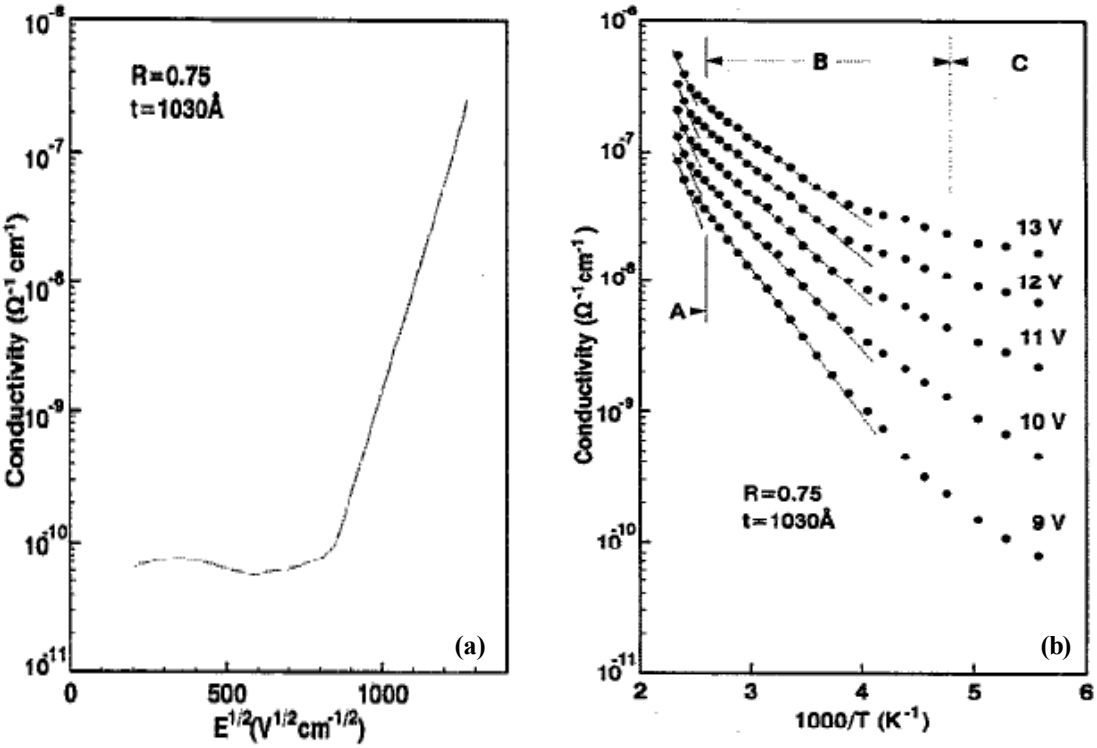

Figure 2.30 a) The Poole-Frenkel plot of the Si-rich PECVD SiN_x:H film measured for a MIM diode at room temperature. **b)** Conductivities of the same film as a function of temperature at constant voltages.[45]

In Figure 2.30 (b), region A shows elevated temperatures above 80 ^{o}C, whereas B is the low temperature region between 80 ^{o}C and -50 ^{o}C. The results of this study are listed in Table 2.6 with comparison to reported values for Poole-Frenkel trap barrier heights (Φ) and zero field conductivity (σ_o) of SiN_x:H films made by the PECVD process. As shown in Table 2.6, the Poole-Frenkel barrier height and conductivity change

with the stoichiometry of films.[45] In particular, when the Si content is increased, the Poole-Frenkel barrier heights decreases, thereby the conductivity increases.

Table 2.6 Poole-Frenkel barrier heights and σ_o values for various compositions in PECVD SiN_x:H films.[45]

	High temperature		Low temperature		
SiN_x	Φ (eV)	σ_0 (Ω cm)$^{-1}$	Φ (eV)	σ_0 (Ω cm)$^{-1}$	Reference
$SiN_{0.7}$	1.15	$(4–40)\times10^{-4}$	0.48	$(0.7–10)\times10^{-7}$	12
$SiN_{1.18}$	1.14		0.93		13
$SiN_{1.0}$	1.2				
$SiN_{1.25}$	1.2				
$SiN_{1.3}$	1.4				14
$SiN_{1.33}$	1.3				
$SiN_{1.33}$(CVD)	1.7				
$SiN_{0.84}$	1.12		1.12		
$SiN_{0.95}$	1.22		1.06		15
$SiN_{1.1}$	1.56		1.36		
$SiN_{1.28}$	1.20		0.98		30
$SiN_{0.19}$	0.82	$(4–18)\times10^{-3}$	0.72	$(1–6)\times10^{-4}$	
$SiN_{0.49}$	0.93	$(5–8)\times10^{-3}$	0.69	$(1–3)\times10^{-5}$	Present
$SiN_{0.54}$	1.10	$(5–10)\times10^{-2}$	0.84	$(1–8)\times10^{-6}$	work
$SiN_{0.84}$	1.22	$(9–10)\times10^{-5}$	0.96	$(1–2)\times10^{-6}$	

Fowler-Nordheim tunneling is reported to occur in thin silicon nitride films (<100nm). However, above this thickness, Poole-Frenkel conduction is likely to take place instead. Bosa *et al.*[55] studied electrical conduction in silicon nitride films deposited at 250 ^oC by a PECVD process with thicknesses ranging from 394Å to 578 Å, and reported that they observed Fowler-Nordheim tunneling for N-rich (N/Si=1.63) and nearly stoichiometric silicon nitride films at high fields (>1 $MV.cm^{-1}$). However, they didn't observe tunneling for Si-rich compositions (N/Si=0.96) and reported that Poole-Frenkel conduction was most likely in this case. A Fowler-Nordheim plot is shown in Figure 2.31. Paloura *et al.*[61] also reported Fowler-Nordheim tunneling in ultra thin (80-120Å) stoichiometric silicon nitride films grown in a low-temperature nitrogen glow discharge at a substrate temperature of 250-350 ^oC.

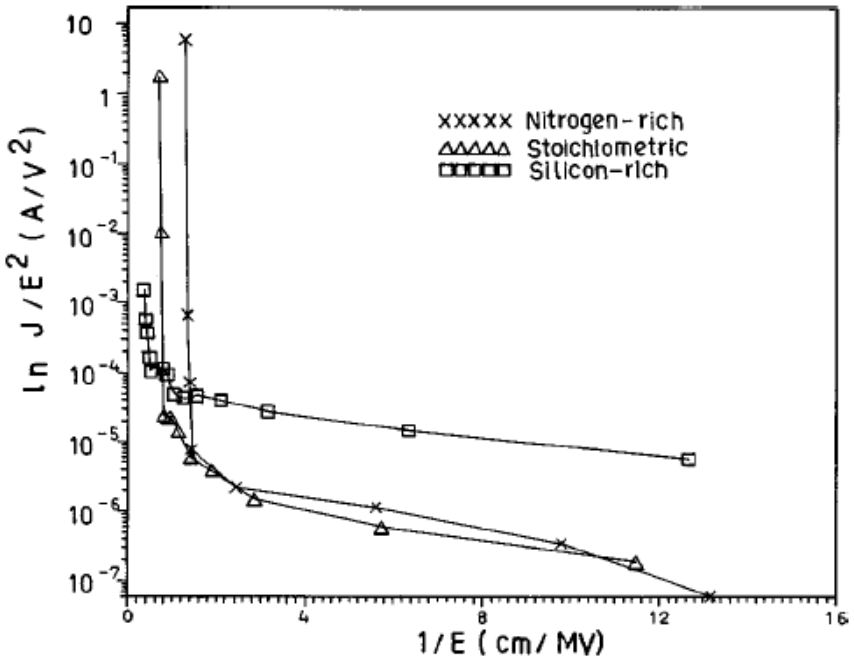

Figure 2.31 Fowler-Nordheim plot of Si-rich, nearly stoichiometric, and N-rich silicon nitride films.[55]

Sze[62] reported that the conduction mechanisms were bulk limited for all field levels in stoichiometric LPCVD silicon nitride films that had thicknesses ranging from 300Å to 3000Å deposited at 1000°C. He concluded that the dominant mechanism was Ohmic at low fields (<2MV.cm^{-1}) and the Poole-Frenkel type at high fields (>4MV.cm^{-1}). Figure 2.32 shows the estimated mechanisms for a Au-Si_3N_4-Mo structure at room temperature in different field regions.[62] Arps *et al.*[63] have proposed the same mechanisms in nitrogen rich PECVD SiN_x:H (x=1.6) films deposited at 350 °C. They stated that the conduction mechanism was Ohmic at low fields (<4MV.cm^{-1}) and Poole-Frenkel at high fields (>4MV.cm^{-1}) for their films. In addition, Masaki *et al.*[45] reported that their silicon nitride films showed bulk limited conduction for all field levels. They reported that the low field (<1MV.cm^{-1}) Ohmic conduction was followed by the high field Poole-Frenkel

conduction (>1MV.cm^{-1}) for 1030Å thick Si-rich PECVD SiN_x:H (x=0.6) deposited at 300 ^{o}C.

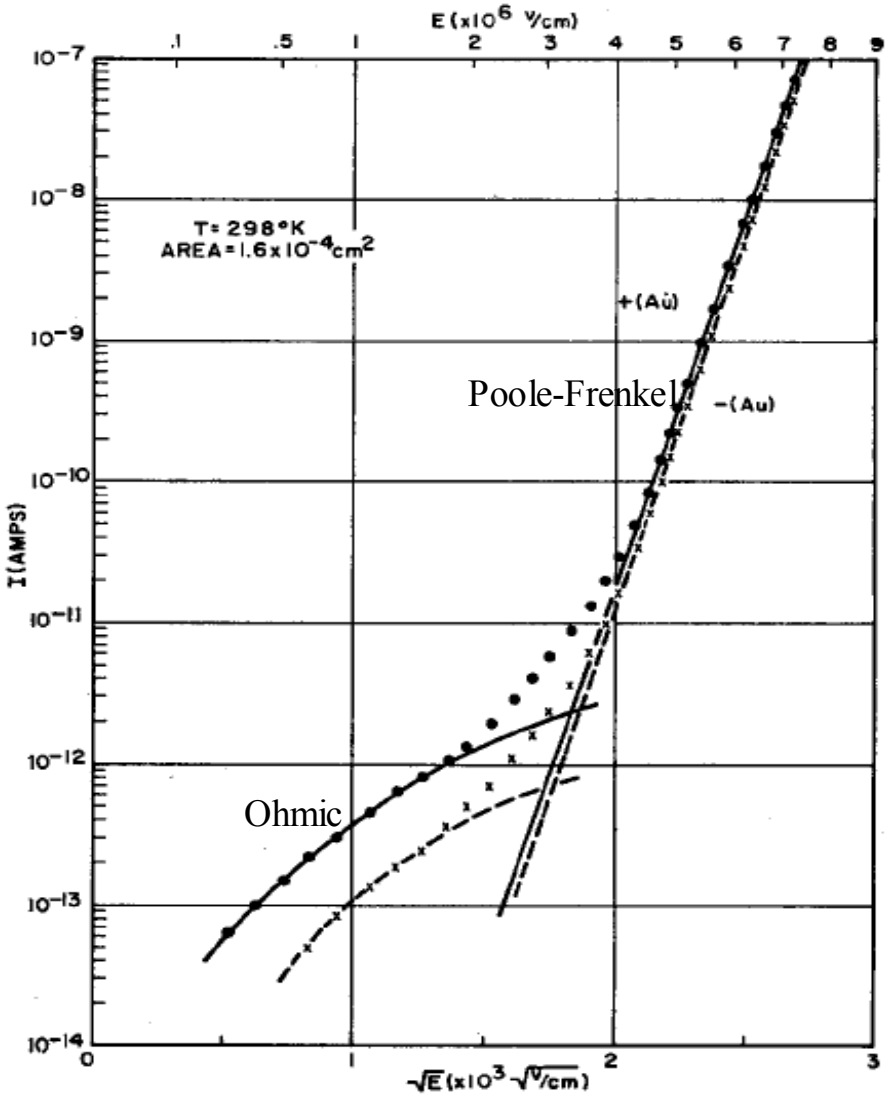

Figure 2.32 Conduction mechanisms in LPCVD silicon nitride films.[62]

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Chapter 3

Experimental Procedure

3.1 Introduction

This chapter summarizes the fabrication and electrical characterization of thin film MIM (metal-insulator-metal) capacitor test structures with silicon nitride as the insulator material. The fabrication steps consisted of patterning and depositing top electrodes. The electrical characterization included DC current-voltage measurements and AC capacitive scans as a function of frequency on these test structures and on MEMS capacitive switches.

3.2 Sample Preparation

In this study, two types of silicon nitride dielectrics (referred to throughout the thesis as Standard and F) were characterized. The wafers (0.25μm-Si_xN_y/0.25μm-Ti-Au/Si_xN_y-barrier/Si-substrate) were manufactured by Northrop Grumman Electronics Systems, Baltimore, MD 21203. The silicon nitride dielectrics were deposited using a PECVD (Plasma Enhanced Chemical Vapor Deposition) process at a temperature of 250 ^oC. The standard and F dielectric were deposited near stoichiometric and Si-rich, respectively. A protective photoresist coating was applied to the wafers after deposition of the dielectric to protect the surface from oxidation prior to metallization. The silicon nitride layer was removed by the reactive ion etching process (RIE) at four or more locations on the wafer in order to open contact paths to the bottom electrode. Before

removing the protective photoresist layer, the wafers were diced using a diamond scriber into small pieces with each piece having a bottom electrode on its edge.

3.3 Lift-off Patterning of Top Electrodes

A lift-off process was used to pattern the top electrodes on the silicon nitride dielectrics. Before starting the photolithography process, the protective photoresist layer was removed by immersing the samples in acetone for 20 minutes and subsequently washing in 2-propanol (IPA) to remove the acetone residue. Subsequently, the chips were dried by blowing nitrogen on the surface of samples. Each piece was baked on a hot plate for 40 seconds at a temperature of 180 ^{o}C in order to remove traces of solvent and moisture from the surface of the sample. LOR5A, (Microchem Chemical Comp., Newton, MA) a lift-off resist, was spun on the sample for 40 sec at 4000 rpm to reach a thickness of approximately 4600Å using a PWM32 photoresist spinner (Headway Research, Inc., Garland, TX). The sample was then baked on a hotplate at 180 ^{o}C for 2 minutes to remove excess solvent. Subsequently, SPR 3012 photoresist, (Shipley, L.L.C., Marlborough, Massachusetts) was spun on the sample at 4000 rpm for 30 seconds with the thickness of approximately 5000Å. The sample was soft baked for 1 minute at 95 ^{o}C to eliminate excess solvent. The process is shown schematically in Figure 3.1. The photoresist was patterned using an MJB3 aligner (Figure 3.2). Typically, an exposure time of 1 minute was used for 2.72 mW power. After exposure, the sample was developed in CD-26 developer (Shipley Company, L.L.C, Marlborough, Massachusetts) for 1 to 2 minutes until the patterns came clean. Patterns for electrodes had areas from $32x10^{-5}cm^2$ to $256x10^{-5}cm^2$.

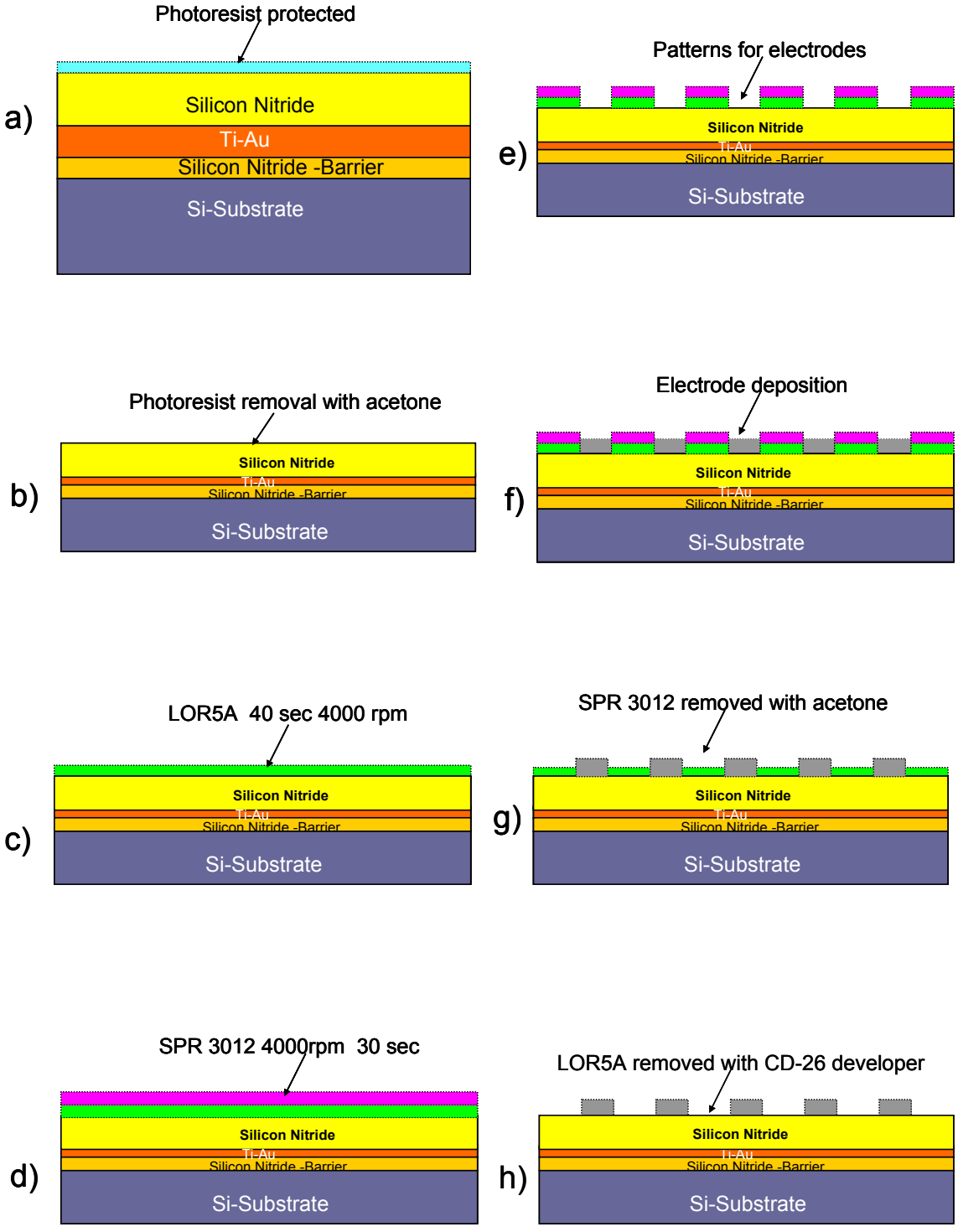

Figure 3.1 Electrode deposition with lift-off process.

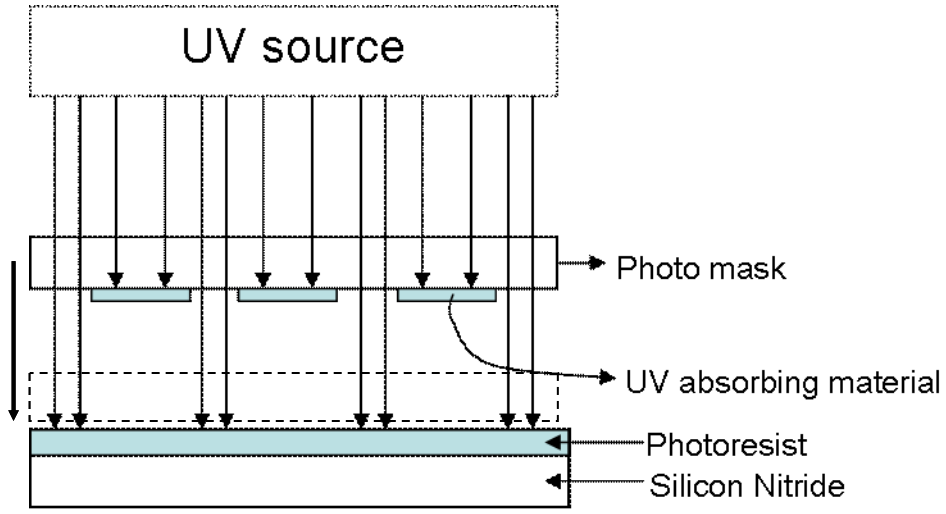

Figure 3.2 Cross-sectional view of exposure process.

3.4 Sputter Deposition of Metal Electrodes

Pt (Platinum), Ti-Au (Titanium-Gold), and Al (Aluminum) metals were chosen as top electrodes because of their work function differences (work functions: Pt, 5.65 eV; Ti, 4.33 eV; Au, 5.1 eV; Al; 4.28 eV).[1] The electrodes were deposited by DC or RF sputtering. Platinum was deposited at 5 mTorr in an argon gas environment for 1000 seconds at a power of 197 watts by DC sputtering at 25 ^{o}C using a Lesker CMS-18 sputtering tool (Kurt J. Lesker Company, West Pittsburgh, PA). Under this condition, the platinum metal electrodes had a thickness of 1500Å. It was found that when the platinum electrodes were deposited at 10mTorr, they had poor adhesion to the silicon nitride. Consequently, a low deposition pressure (maximum 5mTorr) was used for platinum to enhance its adhesion to the silicon nitride. In sputtering, lower pressure leads to fewer collisions of ions and neutral species in the gas phase, and hence increased bombardment of the substrate, enhancing the adhesion of the deposited film[2]. For Ti-Au electrodes, Au was deposited on Ti without breaking vacuum. This was done to prevent oxidation of Ti

on exposure to air. Titanium metal electrodes were deposited at 5mTorr in an argon gas environment by RF sputtering at a power of 200 watts with a DC bias of 470 Volts for 298 seconds at 25 ^{o}C. The Au was deposited by DC sputtering immediately after the deposition of Ti at 5mTorr in an argon gas environment at a power of 200 Watts for 517 seconds at 25 ^{o}C. The resulting thicknesses of the Ti and Au metal layers were approximately 250Å and 1500Å, respectively. Aluminum, 1500Å thick, was deposited in a similar manner. These electrodes were deposited by RF sputtering at 5 mTorr at a power of 200 watts with a DC bias of 370 volts for 3400 seconds at 25 ^{o}C. The deposition conditions are listed in Table 3.1.

Table 3.1 The sputter deposition conditions of electrodes.

Sputtering	Electrode Metals	Thickness (Å)	Deposition pressure (mTorr)	Time (Sec.)	Power (Watt)
DC	Pt	1500	5	1000	197
	Au	1500	5	517	200
RF	Al	1500	5	3400	200
	Ti	250	5	298	200

3.5 Current-Time (I-t) Measurement Modes

Before starting to collect the I-V data, the current-time response of the insulator at constant voltage must be studied to ensure that the measured currents are in the steady-state leakage current region. The current-time response can be measured using three different wave forms:[3]

(I) Staircase mode

(II) Pulse mode

(III) Single step mode

In the staircase mode, the voltage-time profile is a staircase with steps of equal duration.[3] For every voltage step, the current is collected as a function of time. Figure 3.3 shows the profile of a staircase mode, where the circles are the data points that can be taken. In an attempt to reach steady state, the current density at constant field of the standard and F dielectrics was measured as a function of time using the staircase mode for step durations of 16 seconds to 3600 seconds and from 16 seconds to 64 seconds, respectively.

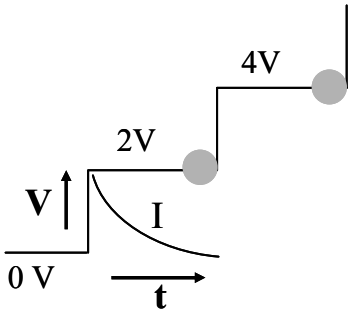

Figure 3.3 Schematic showing the current-time measurement at constant voltage steps using the staircase mode.

In pulse mode, the voltage profile consists of successive steps separated by intervals of the same duration (See Figure 3.4).[3] In this mode, the sample is charged at constant voltage, and then discharged by removing the bias. The data for charging currents and discharging current were collected to separate polarization currents from leakage currents. The current density as a function of time for the standard and F dielectrics was measured using the pulse mode on charging and subsequently discharging

with the same time duration up to 100 seconds. Results were compared to verify leakage current regions.

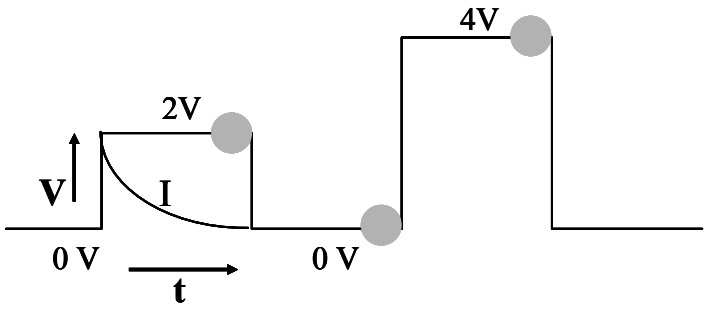

Figure 3.4 Schematic showing the current-time measurement at constant voltage steps using the pulse mode.

In single step mode, for every voltage step, a virgin electrode can be used to collect the data (See Figure 3.5).[3] The purpose of changing the electrode used for each voltage is to eliminate the electric field stress from prior steps. This technique requires longer times than the other techniques to collect the data. This mode wasn't applied to the studied dielectrics for the data collection.

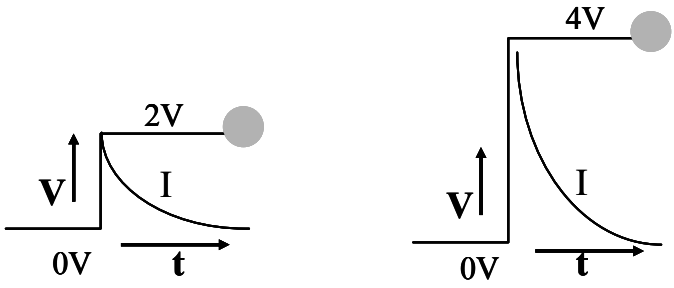

Figure 3.5 Schematic showing the current-time measurement at constant voltage steps using the single step mode.

3.6 Current-Voltage (I-V) Measurements of Silicon Nitride Films

The current–voltage (I-V) behavior of the silicon nitride dielectrics was studied using a 4140B pA meter/DC voltage source analyzer (Hewlett-Packard, Palo Alto, CA) in order to characterize the leakage current and charge trapping behavior in the silicon nitride dielectric as a function of the DC electric field. Figure 3.6 shows a schematic of the I-V measurement set-up. For this measurement, the current input was connected to the top electrode of the sample and voltage was applied to the bottom Au electrode in order to measure the current. The Au electrode was used as the high voltage electrode for all leakage current characterization of the dielectric layers. As top electrodes, Ti-Au, Pt, and Al metals with different work functions were used to understand the effect of the electrode on the leakage current of the dielectric material.

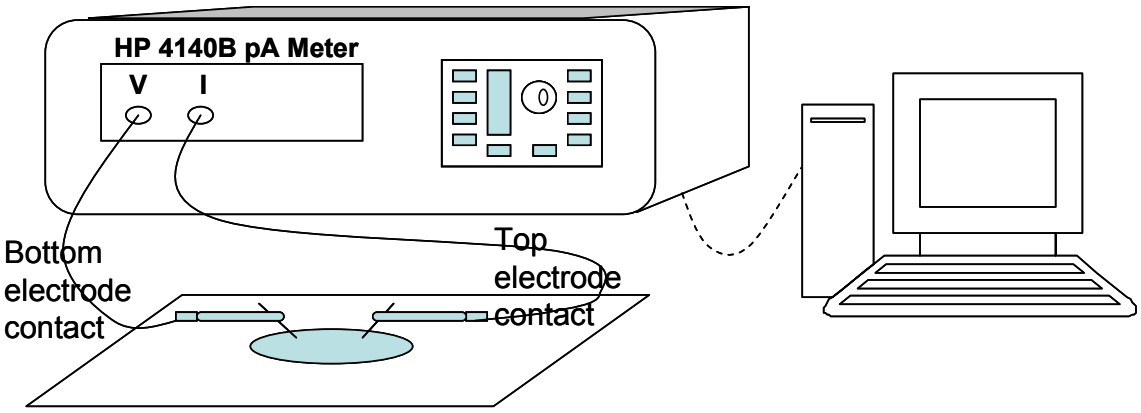

Figure 3.6 Leakage current measurement set-up.

The leakage currents were measured at electric fields from 0kV/cm to 2560 kV/cm. The field was applied for up to 64 seconds at each value in an attempt to reach the DC leakage current conduction regime. The polarity of the applied field was also

reversed by applying either negative or positive voltages to the bottom electrode, and the leakage current of the dielectric was measured.

3.7 Electric Field Stressing of Dielectrics

Silicon nitride dielectrics were stressed at different fields and time frames for two main reasons. First, they were stressed at low fields to observe how fast the relaxation of charges occurred after polarity changes. Second, they were stressed under electric fields for a long period of times to ascertain whether permanent changes were developed in the dielectrics. For these experiments, different virgin electrodes were chosen each time to ensure that the capacitor had no charging history. These measurements were made using different top electrodes (Al, Pt, and Ti-Au). Both standard and F silicon nitride dielectrics were stressed at a negative field of 400kV/cm with respect to the bottom electrode for 1 minute, 10 minutes, and 30 minutes, respectively. The leakage currents were then measured a day later at electric fields between 0 kV/cm and 400 kV/cm. These measurements were repeated by applying a negative field of 400kV/cm for 30 minutes to virgin electrodes and subsequently measuring the leakage current 1 minute, 2 minutes, and 30 minutes after the original bias field was removed at electric fields between 0kV/cm and 600kV/cm. The results were compared to a virgin electrode, which was measured at the same electric fields without prior stressing in order to investigate recovery in the dielectric at lower fields. Figure 3.7 illustrates the polarity of the interfaces and top electrode after charge injection as a cross-sectional view. For the long term study, the standard and F dielectric were stressed at an electric field of 4000kV.cm^{-1} for 23 hours and 2600 kV.cm^{-1} for 1 day, respectively. The current densities of these

dielectrics were measured 1 day later to investigate long term changes in the dielectrics.

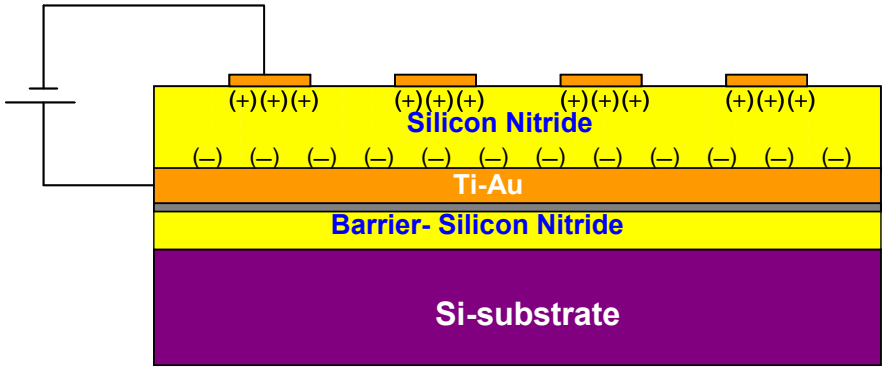

Figure 3.7 Cross-sectional view of a charge injected sample.

3.8 Temperature Dependent Leakage Current Measurements

Temperature dependent leakage current measurements are essential for determining the Schottky barrier height at the electrode-dielectric interface, or the Poole-Frenkel trap barrier height in the bulk of the dielectric. Both Schottky and Poole-Frenkel emission are thermally and field activated processes by which free carriers can be promoted into the conduction band of the insulator.[4] (See equation 3.1 and 3.2 for Poole-Frenkel and Schottky emission for the relation between barrier height, Φ and temperature, T).

Schottky Emission: $$\boldsymbol{J} = \boldsymbol{A} \times \boldsymbol{T}^2 \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \exp(\frac{\beta\sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \qquad (3.1)$$

Poole-Frenkel Emission: $$\boldsymbol{J} = \boldsymbol{E} \times \sigma = \boldsymbol{E} \times \boldsymbol{C} \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \exp(\frac{\beta\sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \qquad (3.2)$$

Pt, Ti-Au, and Al electrodes were used for the temperature dependent measurement of silicon nitride dielectrics. The measurement set up consisted of a heated stage with a k-type thermocouple and the temperature controller. The thermocouple was

used to measure the surface temperature of the stage. The temperature of the stage was set manually using the controller and the thermocouple readout. A computer program written in HP Basic was used to configure, measure, and record the data from a HP 4140B pA meter/DC voltage source analyzer. (This set up is shown in Figure 3.8).

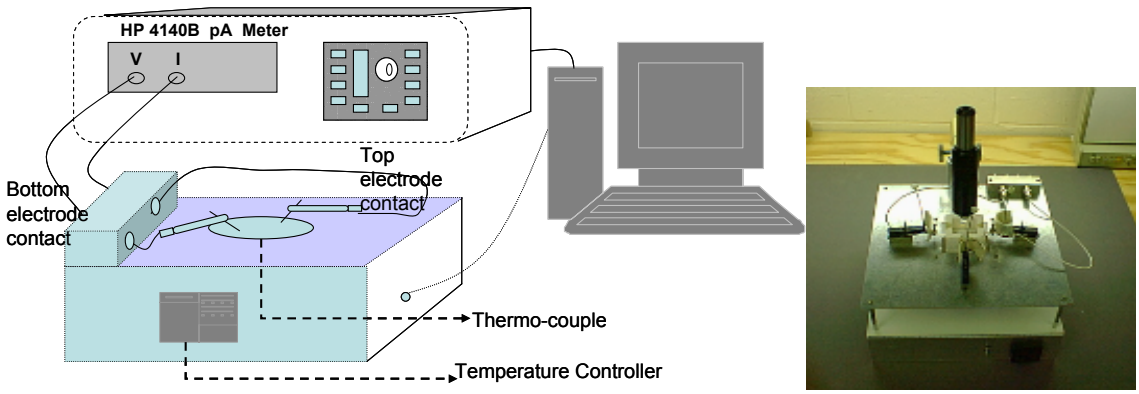

Figure 3.8 The thin film stage set-up used for temperature measurements.

The samples were initially measured at room temperature in order to compare the data with that of the heated sample. The temperature was manually set on the controller to 50^{o}C and was allowed to stabilize for 4 minutes before making the leakage current measurement. While holding the sample at constant temperature, starting at 0 V, the bias was increased in steps of 2V to 58V. This procedure was repeated in steps of 25 ^{o}C for temperatures ranging from 25 ^{o}C to 225^{o}C (<250 ^{o}C deposition temperature) for the F dielectric and from 25 ^{o}C to 275 ^{o}C for the standard dielectric, respectively. These ramping steps are shown schematically in Figure 3.9(a). The activation energy of the emission processes was then determined by plotting the current density as a function of temperature.

It is expected that the current density should increase while heating the sample to high temperatures. For the standard silicon nitride, it was found that on the first heating, the current density for this dielectric decreased below its room temperature (25 ^{o}C) for temperatures between about 50 ^{o}C and 145 ^{o}C. In order to verify whether the current density decrease was caused by electrode failure, the capacitor was cooled to room temperature after each heat treatment and remeasured at the same field. Figure 3.9(b) depicts a schematic of this heating model. In addition, a different method was utilized to probe to this behavior. In this case, a capacitor was first heated to 200 ^{o}C, held for 5 minutes and then cooled to room temperature. 200°C is below the growth temperature, and it was hoped that this would not lead to large permanent changes in the film composition. The temperature dependence of the leakage current was then measured on heating.

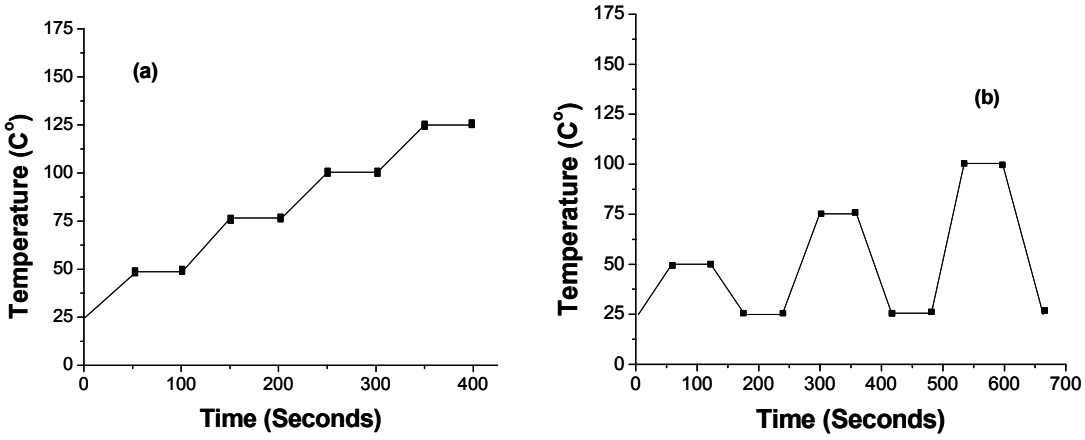

Figure 3.9 Applied ramping models for temperature measurements.

3.9 Current-Voltage Measurement of Capacitive Switches

The primary objective of making all leakage currents measurement on metal-silicon nitride-metal capacitor structure was to investigate the problem of charge trapping in the dielectric of capacitive MEMS switches. As such, it was important to ascertain if the charge injection and leakage behavior in model MIM structures directly applied to the switch, where there is an air gap between the top electrode and the insulator. To get a better understanding of the problem, leakage current measurements were made on capacitive switches provided by Northrop Grumman Electronic Company. The switches were fabricated on quartz and gallium arsenide (GaAs) substrates with F and standard silicon nitride dielectric layers. The thickness of the dielectrics was between 1550Å and 3054Å (Ti-Au/0.25μm-Si_xN_y/Ti-Au/Quartz-GaAs-substrate). A Au/Ti layer was used as the bottom contact under the dielectric layer and Ti-Au bridges of different sizes and shapes were fabricated above the dielectric layer with an air gap. The capacitive switches were closed by applying a bias to the bridge. This causes the bridge to deflect downwards electrostatically, eventually making contact with the dielectric layer. The leakage currents were measured with the bridge in contact. The contact between the bridge, silicon nitride, and bottom electrode was checked with a 4192A HP impedance analyzer (Hewlett-Packard, Palo Alto, CA) by connecting the probe tips to the contact pads at the bridge and the bottom electrode of the capacitive switches before leakage current measurements were made. The leakage current measurements of capacitive switches were carried out using a HP 4140B pA meter/DC voltage source analyzer (Hewlett-Packard Palo Alto, CA).The switches were tested between 0 volt and 60 volts for 64 seconds in steps of 1 volt using ring shaped bridges with the ring area of $5026x10^{-8}$ cm^2. (Pictures of tested

capacitive switches are shown in Figure 3.10).

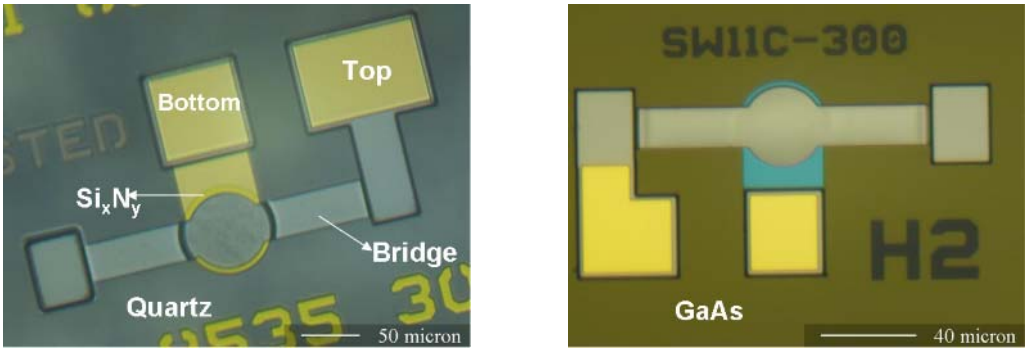

Figure 3.10 Pictures of tested capacitive switches with different substrates.

3.10 Low Frequency Complex Dielectric Constant Measurement

Silicon nitride dielectrics were studied at low frequencies (<1kHz) in order to understand the interfacial polarization response of silicon nitride and its relation to charge trapping. AC signals are one way to investigate the metal-insulator interface. Figure 3.11 shows an ac equivalent circuit of a MIM structure with blocking contacts. The space charge in region 1 and region 2 grows or shrinks with very short or long dielectric relaxation times.

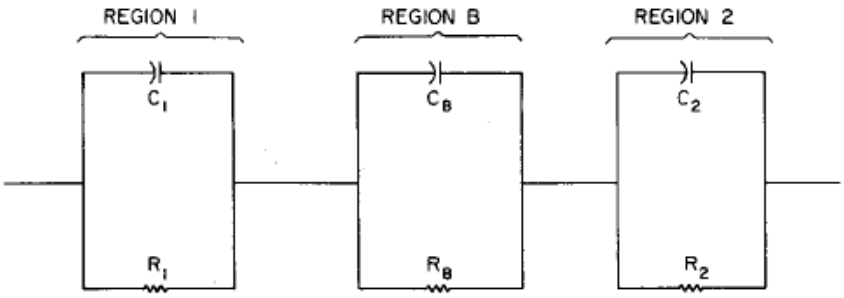

Figure 3.11 Ac equivalent circuit for a MIM capacitor. Region 1 and 2 are first and second electrode metal-insulator interfaces. C_1 and C_2 are the capacitances of the first and second interfaces. Region B and C_B are the bulk region and bulk capacitance. R_1 and R_2 are the resistance of the first and second interfaces. R_B is the resistance of the bulk region.[5]

For the AC signal response of dielectrics, a HP 3562A dynamic signal analyzer (Hewlett-Packard, Palo Alto, CA) was utilized with a low drift charge amplifier to measure the real and imaginary part of the capacitance as a function of frequency. The low drift amplifier[1] was employed for signal amplification due to the small charge output from the capacitor. Figure 3.12 shows a simplified circuit diagram of the low drift amplifier. The collected data were used to calculate the real and imaginary parts of the dielectric constant.

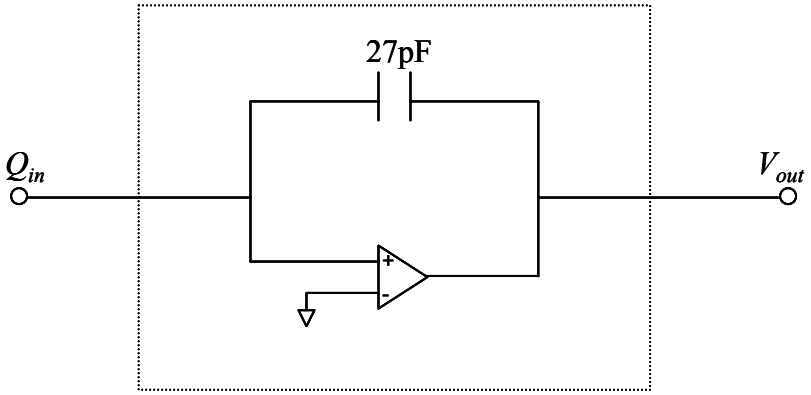

Figure 3.12 Simplified circuit diagram of a low drift charge amplifier.

The input charge (Q_{in}) was amplified to a voltage (V_{out}) via Equation (3.3)

$$V_{out} = \frac{Q_{in}}{C} \qquad (3.3)$$

For the measurement set-up, the output and input of the low drift charge amplifier were connected to the input of the 3562A dynamic signal analyzer and the top electrode of the sample, respectively. The low drift charge amplifier was then brought to zero amps

[1] The amplifier circuit was designed and built by Paul Moses of the Materials Research Institute at Penn State.

to make sure that there was no current flow through the system before running the measurement. The sample was covered with a graphite plate in order to reduce noise that might affect the measurement. The set-up for this experiment is shown in Figure 3.13. Using this set-up, the standard and F dielectric were characterized between 150 mHz and 1kHz at a 1 volt excitation bias.

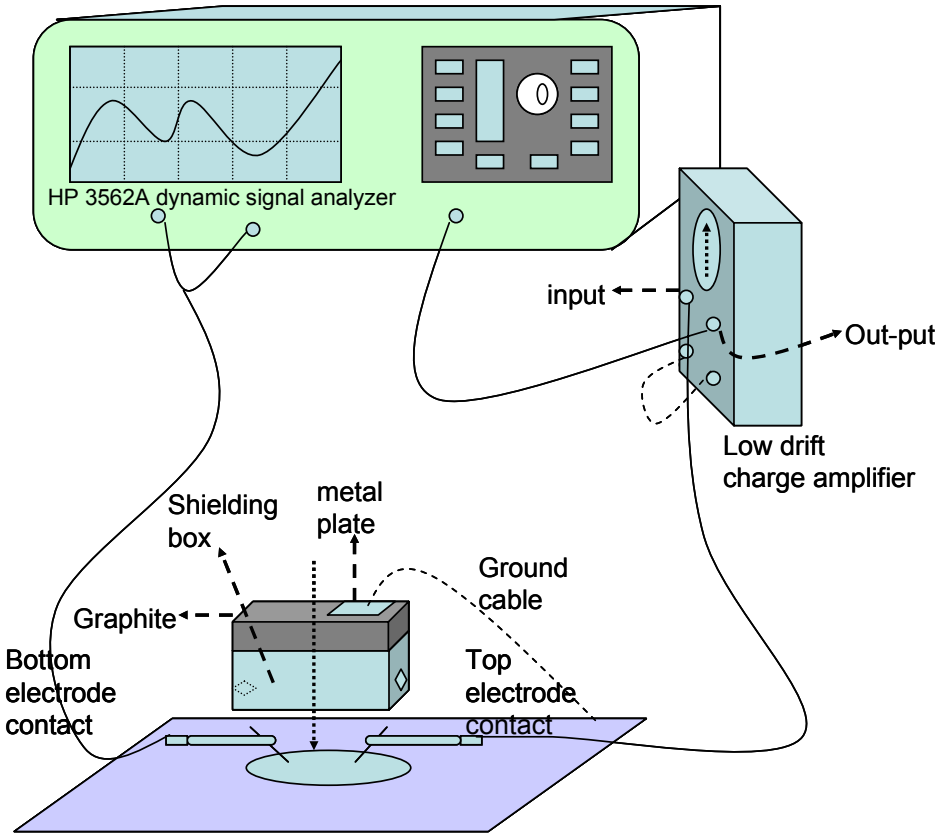

Figure 3.13 Schematic representation of AC measurement set-up.

Charge trapping was also investigated at frequencies between 150 mHz and 1 kHz with a combination of DC and AC measurements. Here, the ac measurement was repeated after dc voltage stressing the dielectric for various times in an attempt to induce

long-lived changes in the dielectric due to charge injection. The dielectrics (F and Standard) were stressed with an HP 4140B pA meter/DC voltage source analyzer (Hewlett-Packard, Palo Alto, CA) at electric field of 2000kV.cm^{-1} for 18 hours and then the AC measurement was carried out a day later on the same electrodes.

3.11 References

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Chapter 4

Results and Discussion

4.1 Introduction

This chapter summarizes results of the current voltage (I-V) and the complex dielectric constant measurements made on MIM (metal/Si_xN_y/metal) capacitors. The current-voltage characteristics of different silicon nitride films were studied using metal electrodes with different work functions to understand the charge transport mechanisms under different conditions. It is hoped that understanding this will improve understanding of charge trapping phenomena in the capacitive MEMS switches. In particular, it was hoped that an understanding of how charge was injected into the dielectric, and how it detrapped would be helpful in suggesting avenues for improving reliability in capacitive MEMS switches.

4.2 Time Dependent Currents

Time dependent measurements of dc current conduction at a constant dc bias must be studied before making any conclusions on the dominant conduction mechanisms in a dielectric. Under a constant applied voltage, the current-time (I-t) response of a dielectric is determined by the following mechanisms: the polarization currents due to stored charges; the steady-state leakage currents due to the charges that are transported between electrodes; and the resistance degradation currents (slow) or breakdown currents (sharp and fast) due to the resistance failure of the dielectric.[1] Figure 4.1 is a schematic of current-time behavior at a constant dc bias in a typical insulator. The initial current decay

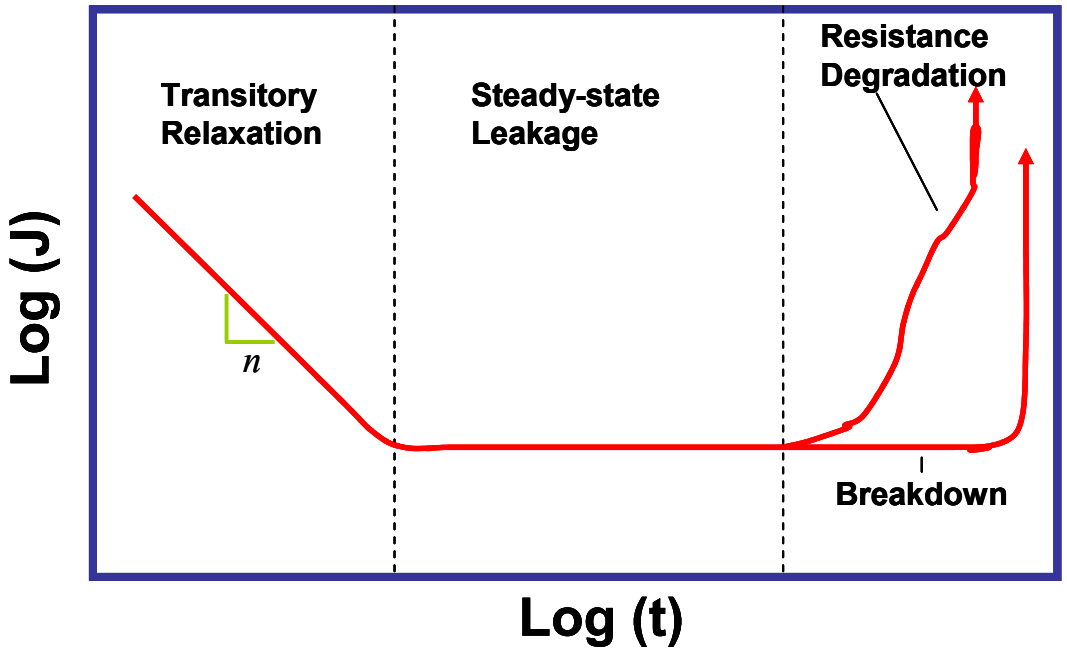

Figure 4.1 Current as a function of time observed in an insulator.[1]

(polarization current) is due to dielectric relaxation. The true leakage currents are determined from the steady-state current region at a constant dc bias. The total charging currents ($J_{Charging}$) flowing through the dielectric at any voltage can be expressed as the sum of the true leakage current ($J_{Leakage}$), and polarization current ($J_{Polarization}$).[2]

$$\mathbf{J_{Charging}(t) = J_{Leakage}(t) + J_{Polarization}(t)} \qquad (4.1)$$

The last region on Figure 4.1 indicates two types of failure in the insulator. The first type of failure is due to resistance degradation. At higher electric fields and temperatures, the current density increases due to creation of additional charge carriers or changes in the heights of any barrier to conduction in the system. As a result, the electrical resistance drops. Further increases in electric fields or temperatures can lead to the failure of the

dielectric. The second type of failure is the breakdown of the dielectric (often yielding a sharp and fast increase in the current). This process also can occur shortly after the polarization region so that the dc leakage current region is not observed.[3]

The relaxation of the currents with time can be described by a power law time dependence (t^{-n}, $n<1$) know as the Curie-von Schweidler law.[4] This describes the linear, non-hysteretic, time-dependent polarization in a dielectric.

$$J_p = \beta t^{-n} + \varepsilon_o E_0 \chi_\infty \delta(t) \qquad (4.2)$$

where β is the polarization current prefactor, $\delta(t)$ is the polarization current spike, and χ_∞ is the high-frequency susceptibility. Using the time dependent part of this equation ($J_p \propto \beta t^{-n}$), a plot of log (J_p) versus log (t) gives a linear relation with the slope of "n".

At this point, it is important to define how the slope changes with time at constant DC bias. For better understanding, this phenomenon is illustrated in Figure 4.2. Under a constant applied electric field, different materials show different relaxation behaviors with different slope values (n). When the linear fitting gives a slope value of zero, it means there is no time dependence. It is usually preferred to study samples under conditions where n-values are close to zero for steady-state leakage currents and smaller than one but not close to zero (due to true leakage current effect) for polarization currents. Slopes larger than one correspond to very fast polarization currents, which are on the order of nano seconds or less.[5] Hence, they become more difficult to detect when their values move to larger numbers ($n>>1$). When n is between zero and one, and is not close to zero, the currents relax slowly to reach the steady-state or never reach this state.[6]

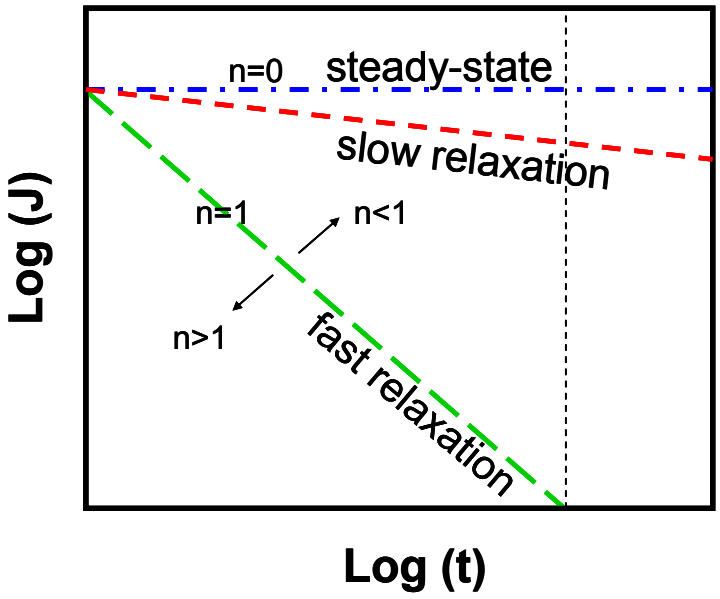

Figure 4.2 The slope of current density changes with time.

The current-time responses of thin film silicon nitride dielectrics (standard and F dielectrics) with different compositions were measured to identify if the current densities reach steady-state. Hence, the first type of analysis was carried out by looking at the deviation in slope values from the relaxation current (time dependent) to the steady-state leakage current (time independent) region.

In 0.25 μm thick F dielectric films, the current density (J)–time (t) response was measured at field levels of 0-2500kV/cm at room temperature. Figure 4.3 (a-c) shows the current-time response of these films at various applied voltages. The slopes are calculated for each applied voltage to observe the transition between different regimes via the slope change (n=slope). As can be seen, the currents are close to the steady-state leakage current regions at higher fields (slope values ≈ 0). At lower fields, the F dielectrics obey a power law time dependence. Hence, a plot of log (J) versus log (t) gives a linear relation that describes the currents in these field regions.

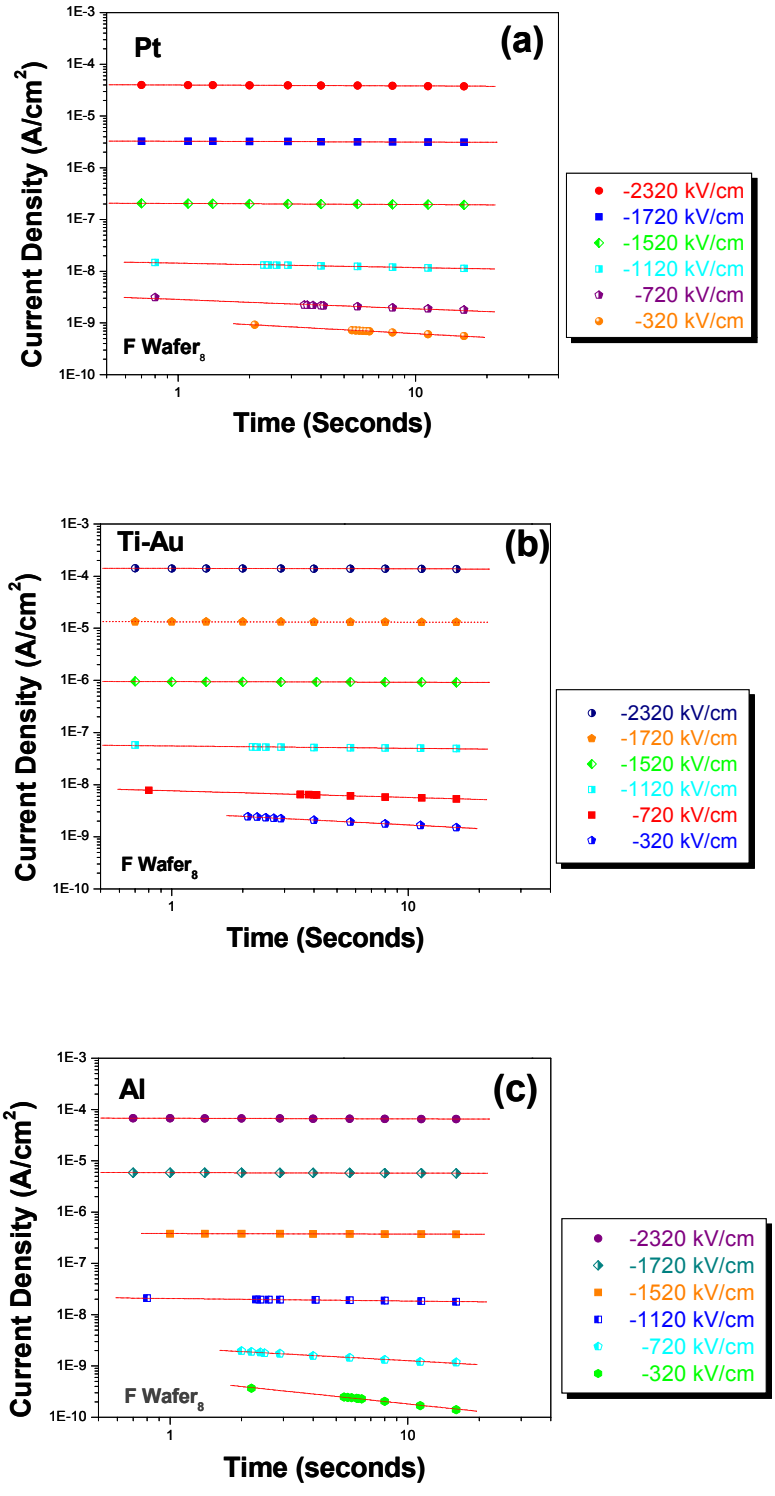

Figure 4.3 (a-c) Current-time response using Pt, Ti-Au, and Al electrodes /0.25µm F-Si_xN_y/Au.

According to the slope values obtained at various voltages, the F dielectric should be treated differently in three regions. At low fields (0-720kV.cm^{-1}), the polarization current dominates. At intermediate fields (720-1000kV.cm^{-1}), the behavior is a mixture of steady-state leakage and polarization current, and at higher field ($\geq$1000kV.cm^{-1}) as a true leakage current contribution.

In Figures 4.4 (a-c), the log (J) versus log (t) response is shown for different top electrode metals for a 0.25μm standard silicon nitride. Several features should be noted. First, the magnitude of the current densities of the F and the standard dielectrics are comparable at low fields. However, the current density of the standard nitride remains small, even at high bias fields. Secondly, in contrast to the F dielectric, thin films of the standard Si_xN_y dielectric have current-time responses that obey a power law at all field ranges investigated (0-2320 kV.cm^{-1}). Hence, the current-time response of this dielectric is dominated by polarization currents over the entire field range investigated. Tables 4.1 and 4.2 summarize the slope values of both dielectrics with different metal electrodes.

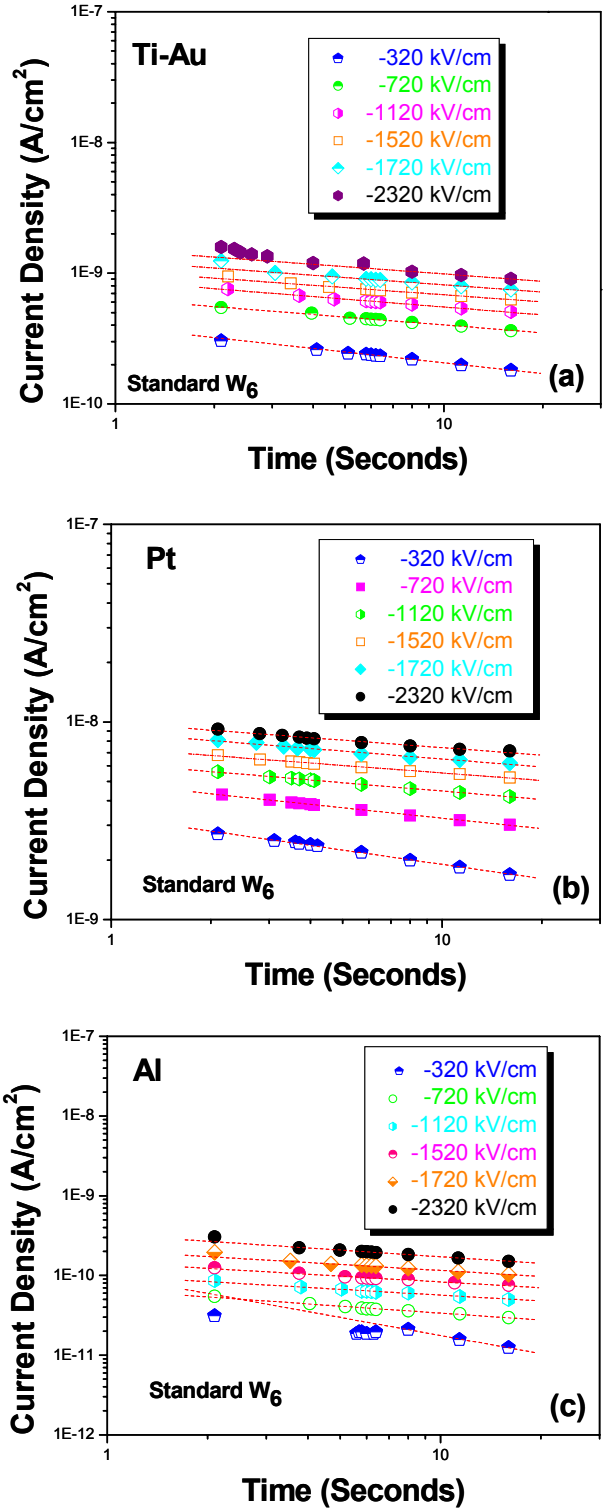

Figure 4.4 (a-c) Current-time response using Pt, Ti-Au, and Al electrodes /0.25μm standard Si_xN_y/Au.

Table 4.1 Summary of current-time response for F dielectric with different top electrodes.

F Si_xN_y				
V (Volt)	**E (kV/cm)**	**n/Pt**	**n/Ti-Au**	**n/Al**
-58	-2320	0.018 $\pm 3x10^{-4}$	0.0097 $\pm 2x10^{-4}$	0.020 $\pm 3x10^{-4}$
-48	-1720	0.015 $\pm 4x10^{-4}$	0.0075 $\pm 3x10^{-4}$	0.009 $\pm 4x10^{-4}$
-38	-1520	0.020 $\pm 5x10^{-4}$	0.010 ±0.0002	0.010 ±0.0003
-28	-1120	0.080 ±0.002	0.045 ±0.001	0.050 ±0.002
-18	-720	0.180 ±0.01	0.128 ±0.002	0.250 ±0.003
-8	-320	0.250 ±0.005	0.230 ±0.003	0.500 ±0.02

Table 4.2 Summary of current-time response for standard dielectric with different top electrodes.

Standard Si_xN_y				
V (Volt)	**E (kV/cm)**	**n/Pt**	**n/Ti-Au**	**n/Al**
-58	-2320	0.11 ±0.003	0.18 ±0.003	0.258 ±0.0035
-48	-1720	0.12 ±0.002	0.18 ±0.003	0.250 ±0.003
-38	-1520	0.12 ±0.003	0.18 ±0.002	0.240±0.0032
-28	-1120	0.15 ±0.002	0.20 ±0.005	0.240±0.004
-18	-720	0.19 ±0.007	0.20 ±0.003	0.290 ±0.006
-8	-320	0.25 ±0.002	0.28 ±0.002	0.756 ±0.04

In an attempt to reach the steady-state leakage current region, the standard dielectric was held under an electric field for a prolonged time (3600 seconds) at room temperature. The results are plotted in Figure 4.5 for intermediate and higher fields. As can be seen, these conditions were still insufficient to access the true leakage regime of this dielectric. Indeed, the slope values increased when the standard dielectric was held under electric field for long time. It is possible that if steady-state current densities for this dielectric exist, they should be observed below the detection limit of the equipment ($<10^{-14}$ A/cm^2).

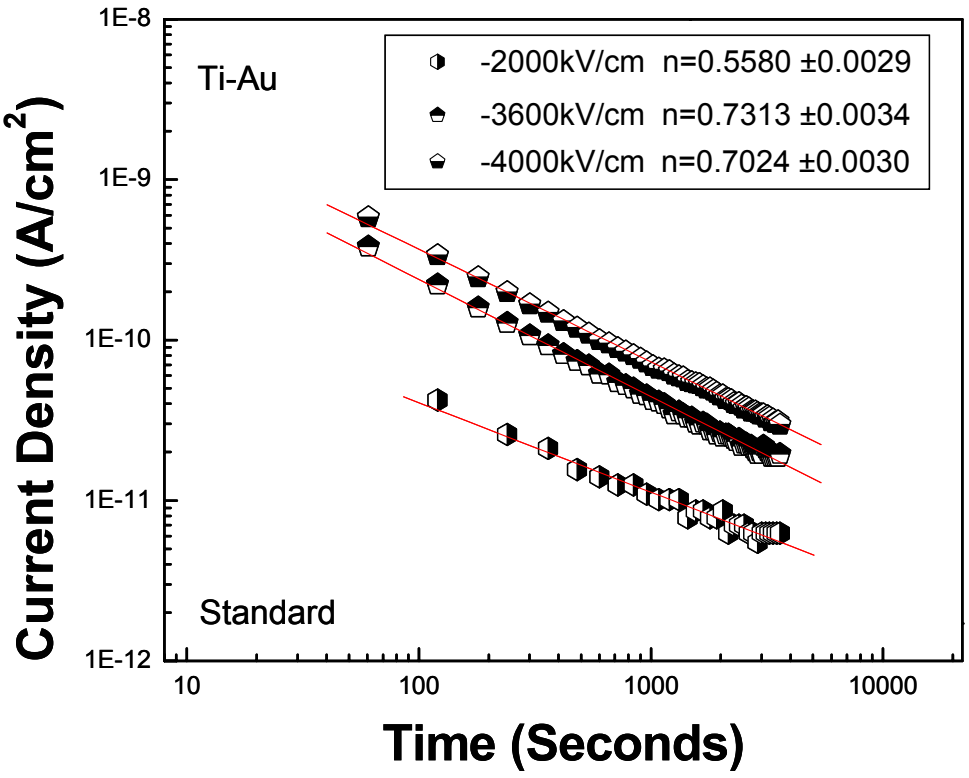

Figure 4.5 Current-time response of a standard dielectric for longer holding time.

As temperature is increased in a dielectric, a higher carrier concentration results. This should increase the leakage current density, simplifying detection of a true leakage

current and study of the conduction mechanisms. Consequently, measurements of the leakage current were made at elevated temperatures.

The leakage current in the F dielectric was studied as a function of the time over the temperature range between 298 K and 423 K at a constant electric field of 2320kV.cm^{-1}. Figure 4.6 shows the results. As seen in Figure 4.6, at these high fields, the current density for all temperatures is essentially independent of the time. These slope values are lower than the values obtained at room temperature.

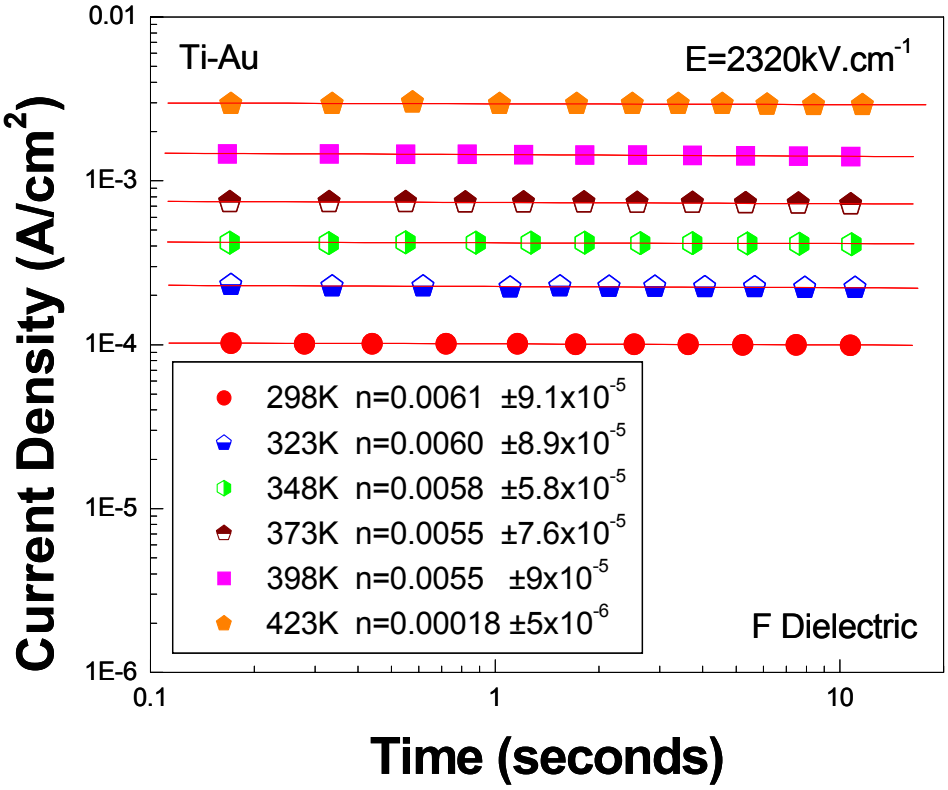

Figure 4.6 Current density-time response in F dielectric for different temperatures.

In the standard dielectric, it was found that the current density did not show a consistent

increase on increasing temperature for the first heating cycle, and that the room temperature leakage current changed after heating (See Fig. 4.7). This was believed to be due to changes in either the film stoichiometry (perhaps due to H evolution) or changes in the electrode/film interface.

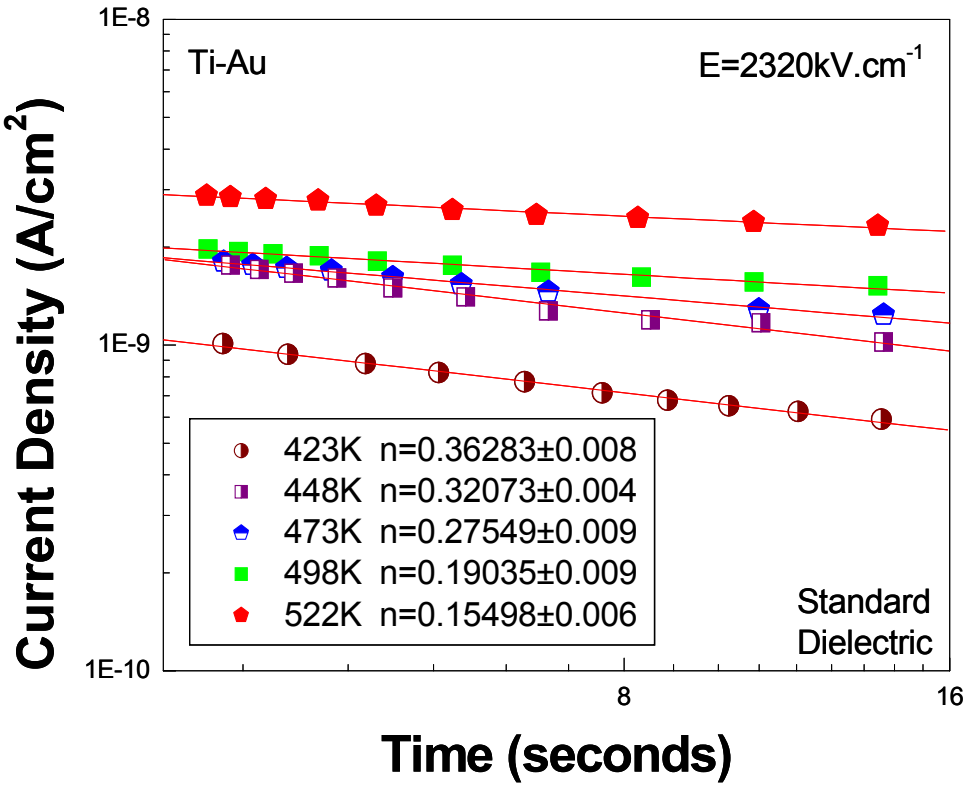

Figure 4.7 Current density-time response in the standard dielectric for different temperatures.

4.3 Current-Time Analysis Using Pulse Mode

In the previous sections, the time dependent results were interpreted based on the time dependence of the charging currents at constant DC bias. In order to confirm the results, additional measurements were carried out by charging (constant DC bias) and discharging (zero bias) of the capacitors. In the absence of an electric field (after

charging), the discharging current density ($J_{Discharge}$) is equal to the polarization current density ($J_{Polarization}$), but with opposite sign. [2,6]

$$J_{Polarization}(t) = -J_{Discharging}(t) \qquad (4.3)$$

Using equations 4.1 and 4.3, the leakage current density is equal to the difference between the charging and discharging current density responses given by[2]

$$J_{Leakage}(t) = J_{Charging}(t) - \left|J_{Discharging}(t)\right| \qquad (4.4)$$

Figure 4.8 shows the current density–time measurements of the standard dielectric that

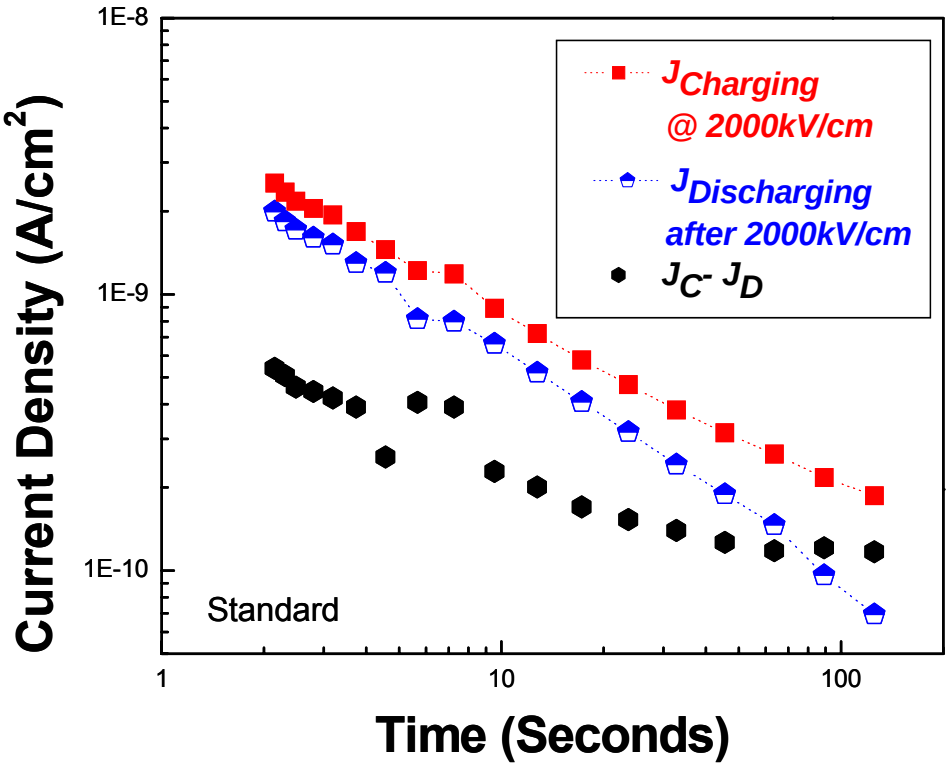

Figure 4.8 The charging and discharging current density-time response in the standard dielectric.

was made on charging and discharging. In this dielectric, the current density for discharging is approximately equal to the current density for the charging. Thus, the leakage current density is found to be small. According to equations 4.3 and 4.4, in the

standard dielectric, polarization currents are dominant at room temperature at electric fields ≤2000kV.cm^{-1}. This is consistent with the observed time dependence of the leakage current density at constant electric field. Moreover, Figures 4.9 (a-b) show the charging

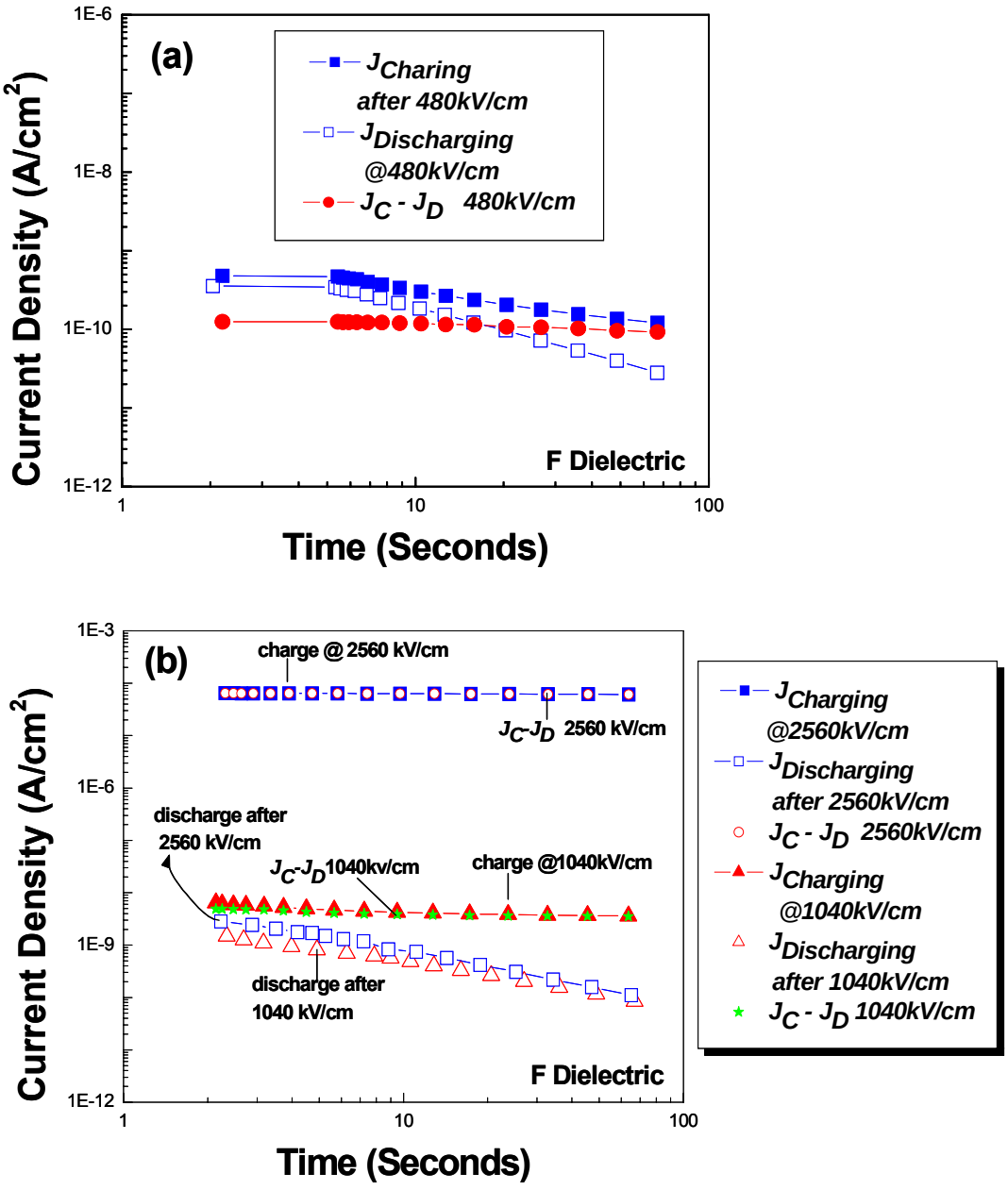

Figure 4.9 (a) The charging and discharging current density–time response at 480 kV.cm^{-1} in the F dielectric. **(b)** The charging and discharging current density–time response in the F dielectric at 1040 kV.cm^{-1} and 2560 kV.cm^{-1}.

and discharging current density response in the F dielectric. By comparison, for the F dielectric, the discharge current density is reasonably close to the charging current density at lower fields. However, the situation changes dramatically at higher field levels. Indeed, the differences between the charging current densities and discharging current densities (J_C -J_D) are approximately equal to the charging current densities at higher fields. Hence, DC leakage currents dominate the charging currents at higher fields. Again, this is consistent with the leakage-time data.

4.4 Current-Voltage Response in MIM Capacitors

When a voltage is applied to a dielectric between two electrodes (MIM capacitor), the conduction process is dependent not only on the type of electrode or the insulator but also on the contact that forms at the interfaces.

When a metal and an insulator are brought into contact, the energy band structure changes, in some cases forming barriers that control the carrier flow. The conduction processes thus can be categorized into two groups[7]: I) bulk-limited conduction, II) electrode-limited conduction. At the metal-insulator interface, three types of contacts can exist[8]: 1) Ohmic contact (bulk limited): The conduction of carriers isn't limited by a barrier at the interface; thus the conduction of carriers depends on the bulk properties of the dielectric. 2) Blocking (Schottky) contact (electrode limited): The conduction of carriers is blocked by a barrier at the interface; thus the conduction of carriers depends on the metal electrode work function. 3) Neutral contact: this is a transitional behavior between ohmic and blocking contacts; thus the conduction of carriers depends on both contributions. In addition, this contact type assumes that the insulator is intrinsic; thus

there is no dominant charge carrier in the insulator (the number of holes is equal to the number of electrons)[7-8]. Figure 4.10 shows the possible contacts that might exist at a metal-insulator interface after contact at equilibrium. The contact issues above play an important role in the I-V response when the field is applied to the MIM capacitor. Contacts can also be affected by structural defects in the material. Such defects are commonly observed in low-temperature CVD (chemical vapor deposition) silicon nitride where some of the bonds are broken (dangling) and can influence current flow in the insulator. These dangling bonds are thought to act as centers for trapping or detrapping of carriers in silicon nitride under electric field stress.[9]

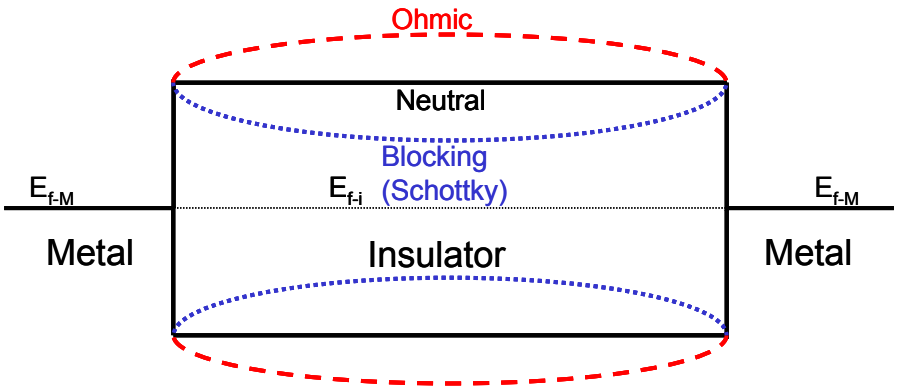

Figure 4.10 Types of contacts that exist at a metal-insulator-metal interface after contact at equilibrium.[7-8]

As mentioned in Chapter 3, in this work, the effect of different top electrodes on the current transport in the silicon nitride films was studied. Assuming there are no defects or trapped charges in the film or at the interface between the film and the electrode, the band diagrams for MIM capacitors with different top electrodes (Pt, Ti-Au, and Al) and a Au bottom electrode are illustrated at thermal equilibrium, based on the neutral contact for each case, prior to contact in Figure 4.11, and after contact in Figure 4.12.

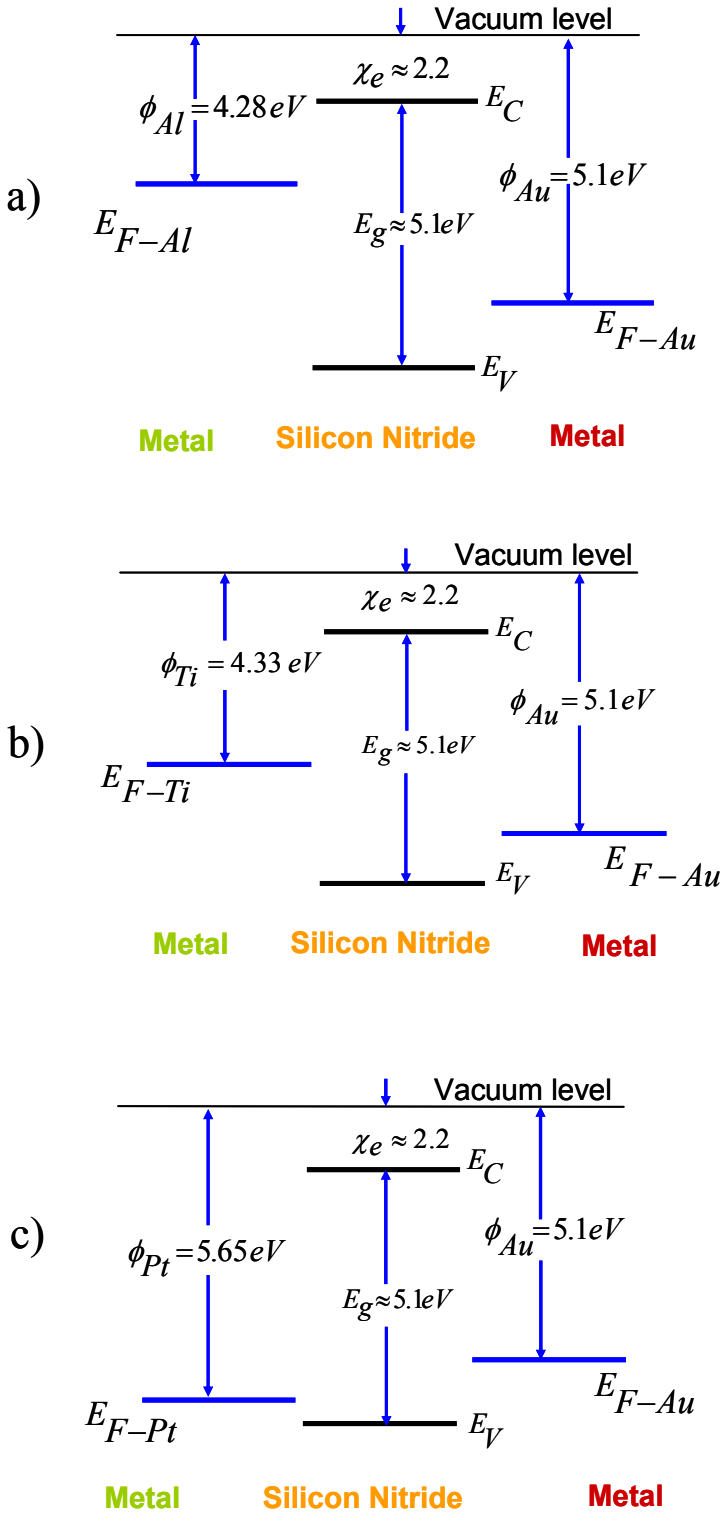

Figure 4.11 Energy band diagrams for silicon nitride MIM structures prior to contact with different top electrodes.

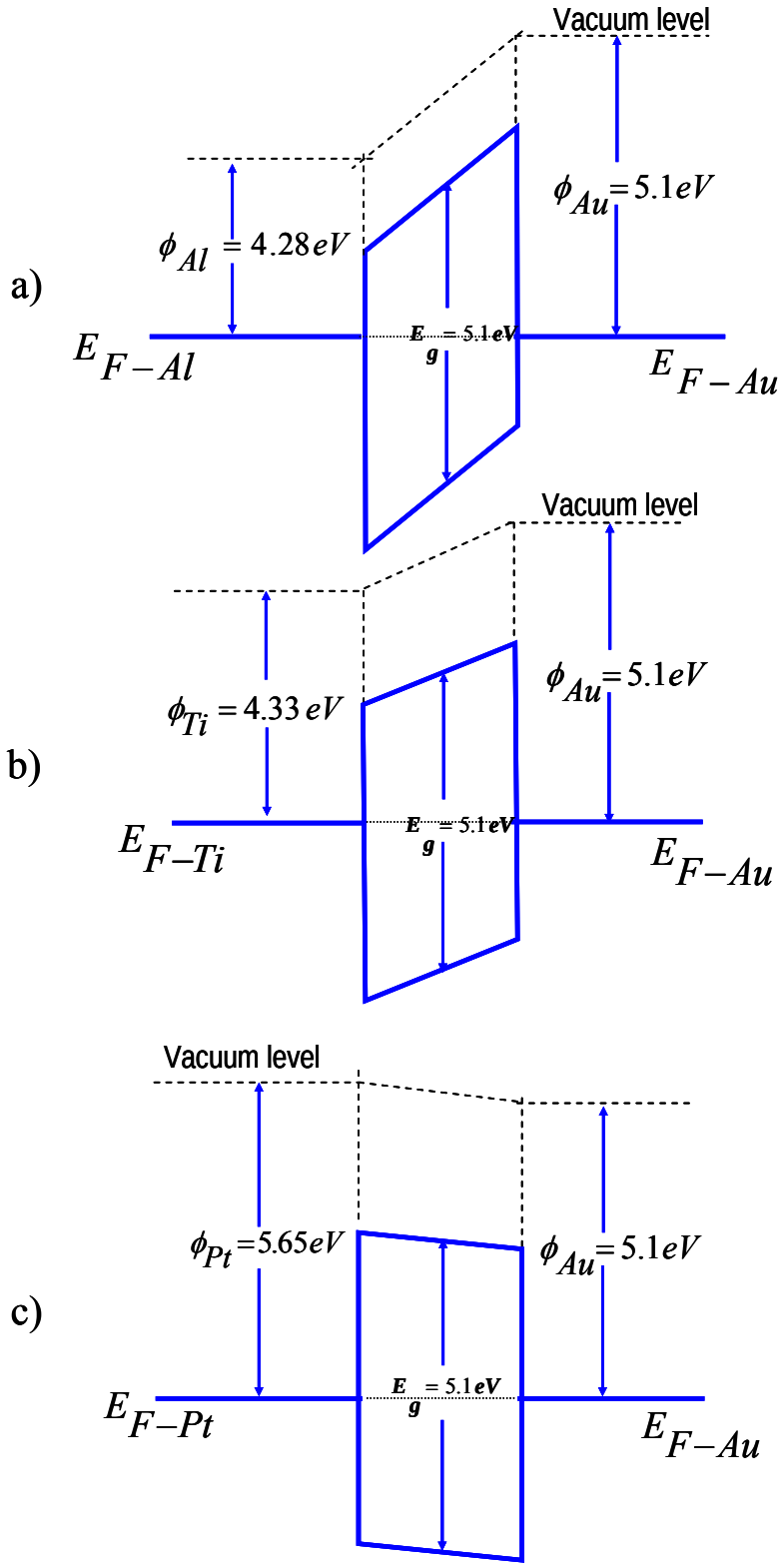

Figure 4. 12 Energy band diagrams for silicon nitride MIM structures at thermal equilibrium after contact with different electrodes.

The band gap energy (E_g) and electron affinity (χ_e) used for the stoichiometric silicon nitride dielectric were 5.1and 2.2 eV, respectively.[10,11] These values are applicable only for stoichiometric silicon nitrides. Figure 4.13 shows the optical band gap energy changes as a function of the N content in a-SiN_x:H (hydrogenated amorphous silicon nitride) films deposited by rf sputtering.[12] It can be seen that the increase in the N content x increases the optical band gap of the a-SiN_x:H. Consequently, the diagrams shown in Fig. 4.11 and 4.12 should be modified somewhat for the F dielectric, since it is silicon rich.

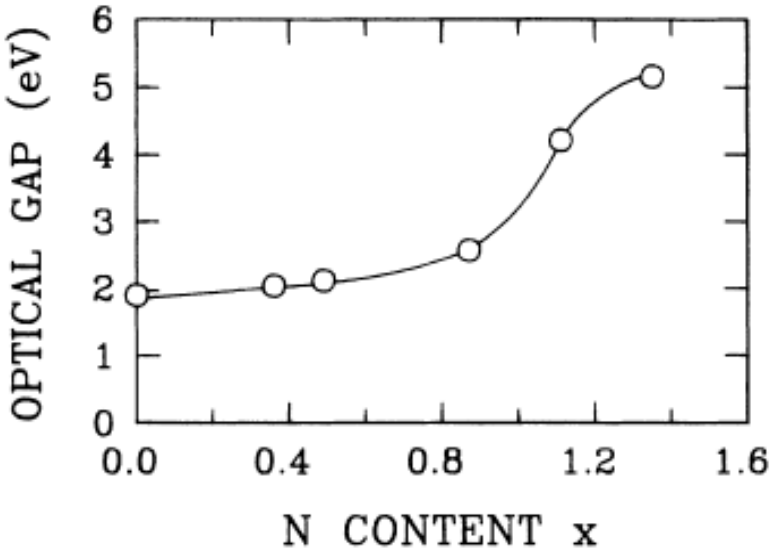

Figure 4.13 Optical band gap (E_g) as a function of the N content (x) in the a-SiN_x:H.[12]

The work functions (ϕ) for Al, Ti, Au, and Pt electrode were taken to be 4.28 eV, 4.33 eV, 5.1 eV, and 5.65 eV respectively.[13] As shown in Figure 4.12, asymmetric contacts should be taken into consideration in the calculation of the barriers for electron transport in an insulator.[7-8] At equilibrium, the work function differences between Al and Au electrodes; Ti and Au electrodes; and Pt and Au electrodes are computed to be 0.82 eV, 0.77eV, and

0.55eV respectively for MIM capacitors. Hence, one can expect the current density for these capacitors to be inversely proportional to the work function differences between bottom and top metal electrodes if the current density is contact limited.[7-8] This would suggest that the measured current densities should be lower for Al/Si_xN_y /Au capacitors, intermediate for Ti/Si_xN_y/Au capacitors, and higher for Pt/Si_xN_y/Au capacitors.

As shown in Figure 4.14, a standard silicon nitride dielectric was measured under applied electric fields up to 2000kV.cm^{-1} with Al, Ti-Au, and Pt top electrodes (Au bottom electrodes). The measured current densities were higher for Pt top electrodes,

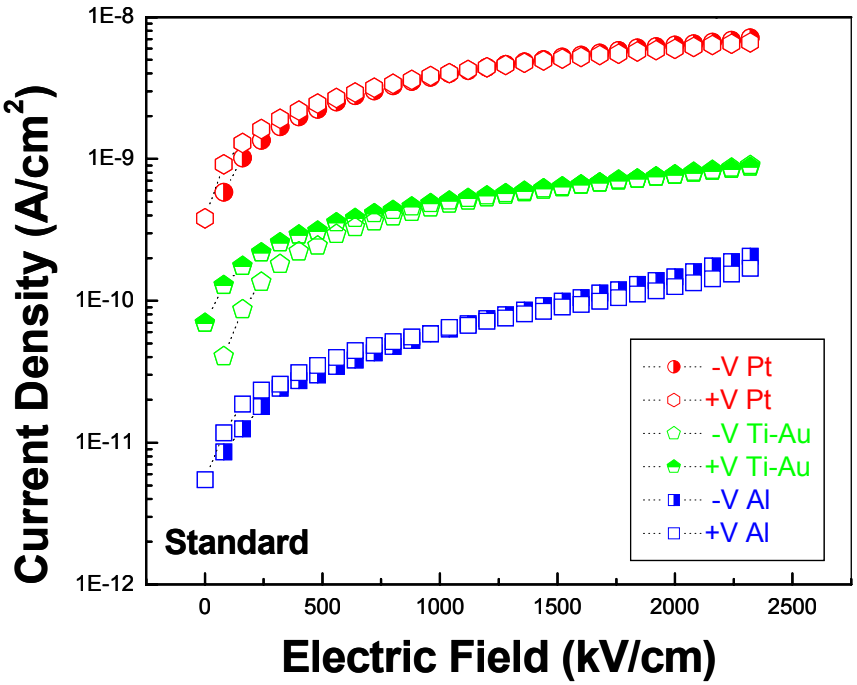

Figure 4. 14 The comparison of the current densities in a standard dielectric with Al, Ti-Au, and Pt electrodes.

intermediate for Ti-Au, and lower for Al top electrodes for measurements made 16 seconds after application of voltage. However, as described before, these measurements

were made in the polarization current regime, so these are not true leakage currents. The results do suggest that the total current is affected by the contact. Additionally, as seen in Figure 4.14, the current density of the standard silicon nitride was measured as a function of the applied electric field for both negative and positive bias for Pt, Ti-Au, and Al top electrodes. From the figure, it is clear that there is no change in the current densities with the polarity of the bias voltage (for fields below $\leq$2320kV.cm^{-1}).

As depicted in Figure 4.15, in the F dielectric, there is no strong correlation between the measured current density and the work function difference of the electrodes. This may be either because the conduction is controlled more by the bulk rather than the electrode interface in this dielectric, or because defect states in the dielectric cannot be ignored, as in the simple picture shown in Figs. 4.11 and 4.12.

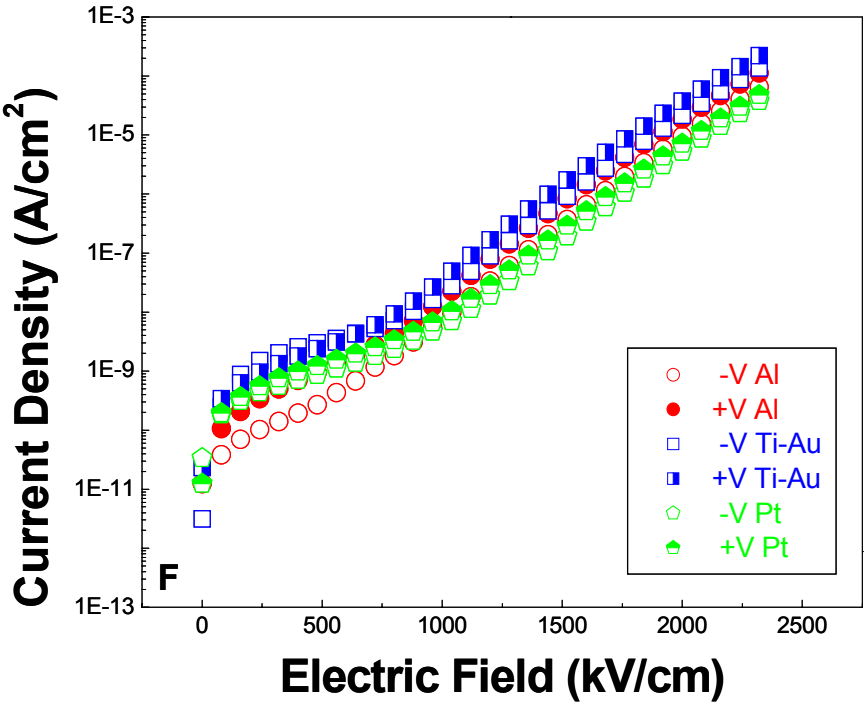

Figure 4. 15 The comparison of the current densities in F dielectric measured with Al, Ti-Au, and Pt electrodes.

In the F silicon nitride films, as shown in Figure 4.16, the observed current density is much higher than that for the standard dielectric. In addition, the current density increases

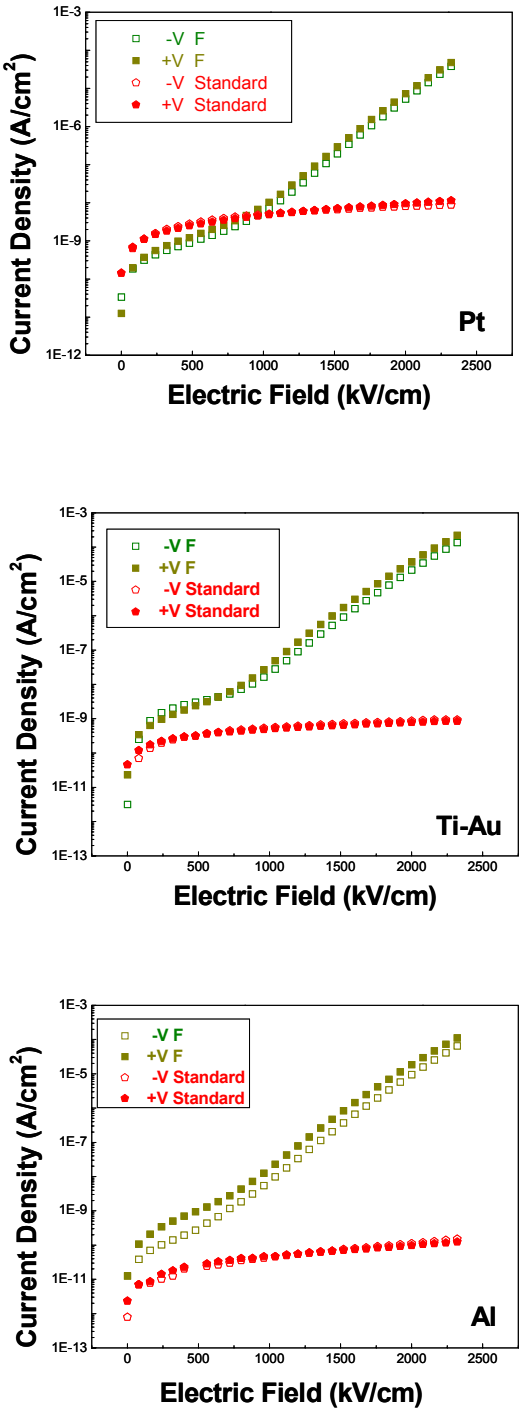

Figure 4.16 The current density comparison of the standard and F dielectric.

significantly at electric fields greater than 750kV.cm^{-1}, reaching J = 10^{-4}A.cm^{-2} at an electric field of 2320 kV.cm^{-1}.

Habermehl *et al.*[14] also investigated charge transport phenomena in silicon-rich, low stress silicon nitride thin films ranging in composition from $SiN_{1.33}$ to $SiN_{0.54}$ prepared by a low pressure chemical vapor deposition (LPCVD) technique. They concluded that at high electric fields, the conduction mechanism was best described as Poole-Frenkel. Their Poole-Frenkel plot is depicted in Figure 4.17. It was found that by

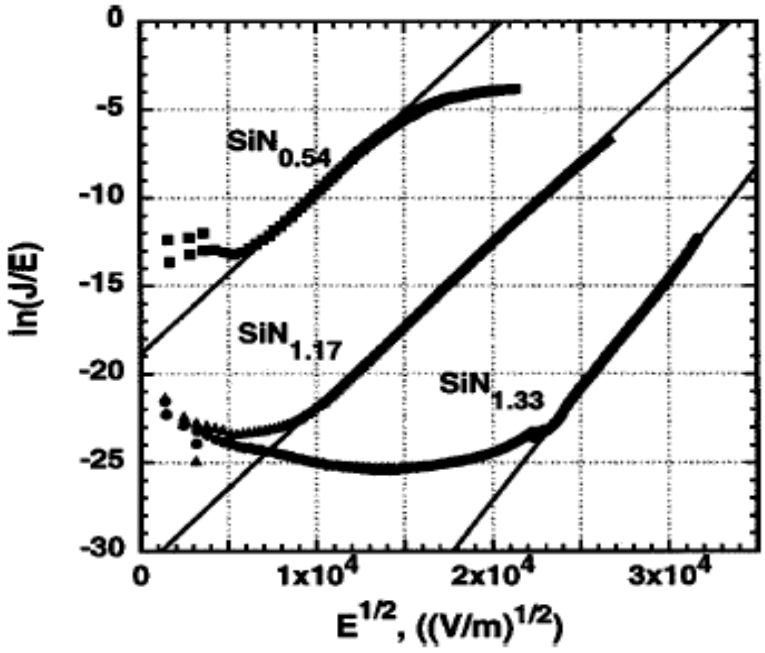

Figure 4.17 Poole-Frenkel characteristic at 298K for various film compositions.[14]

increasing the Si content in the silicon nitride, the current density increased by about seven orders of magnitude. This suggests that the electrical characteristics of the F dielectric are consistent with Si-rich behavior.

4.5 Air Exposure of the Silicon Nitride Surface

In order to investigate whether or not the surface cleanliness of the silicon nitride film affected the current transport behavior, a standard silicon nitride was deliberately exposed to air prior to deposition of the top electrode. This presumably might enable a silicon oxide layer to form on the surface. A second wafer was protected by photoresist immediately after deposition, and this protective coating was removed only immediately before the top electrode deposition. Figures 4.18 and 4.19 show the current–voltage measurements carried out on standard and F dielectric films with protection and without protection. It is clear that in the short term the air exposure did not have any significant impact on the electrical properties. That is, the shapes of the current density curves suggest that the same mechanisms control the transport in both cases.

Liao *et al.*[15] reported the post-deposition oxidation of a-SiN_x:H films deposited by PECVD process at deposition temperatures ranging from 50-250^{o}C with flow rates of 3 sccm for pure SiH_4 and 58 sccm for pure NH_3. It was found that after taking the films out of the reaction chamber, they started to react with moisture (H_2O) and formed a chemically stabilized Si-O-Si or Si-O-H bond configuration. Shown in Figure 4.20 are data for a a-SiN_x:H film deposited by a PECVD process at 100^{o}C. The oxidation of this film was measured as a function of the time using infrared absorption spectroscopy. It can be seen that formation of Si-O-Si bonds was observed in the last spectra (1410 minutes). However, when the film was deposited at 225 ^{o}C (yielding a denser structure), the oxide formation due to room temperature air exposure took almost 70 days to consume 10 % of the film. The subtle changes in the leakage characteristics for short-term air exposure suggest that there should be some latitude for contact with moisture in

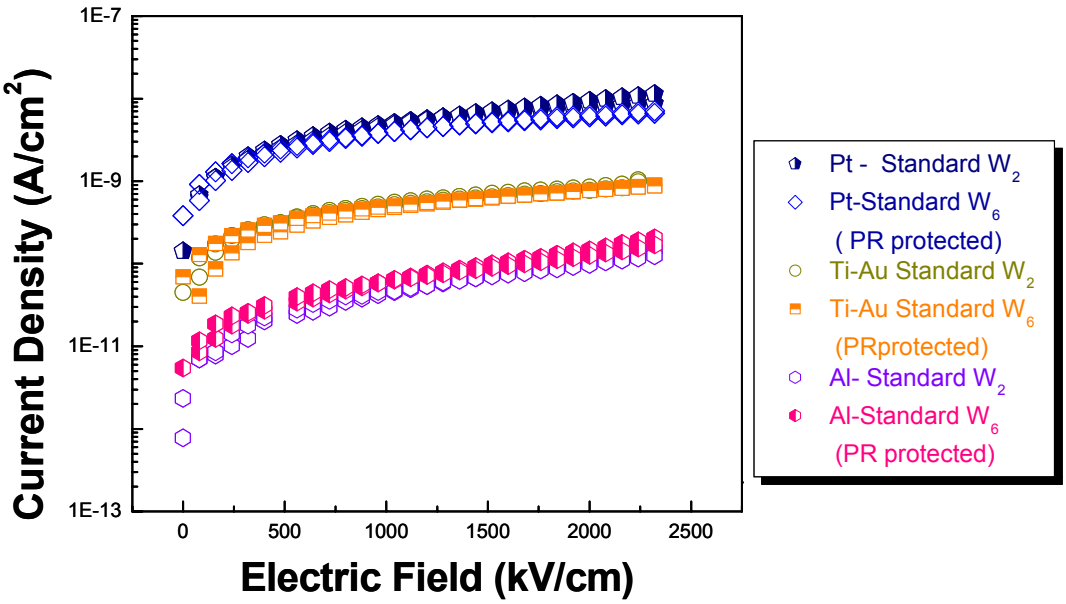

Figure 4.18 Current density versus electric field for the standard dielectrics with photoresist (PR) protection and without protection.

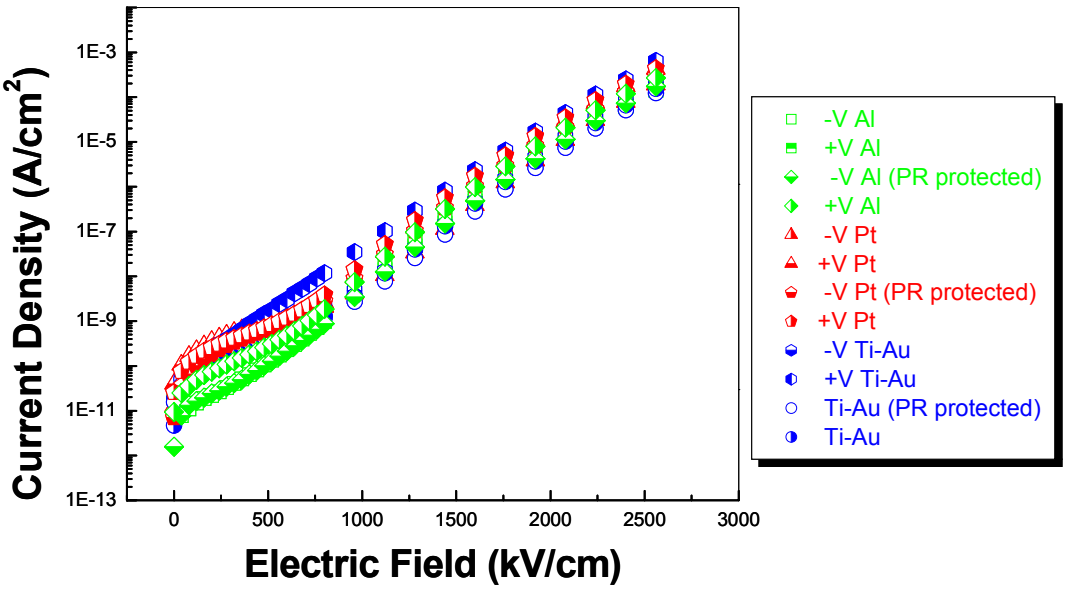

Figure 4.19 Current density versus electric field for F dielectrics with photoresist (PR) protection and without protection.

the process window in the preparation of capacitive MEMS switches using silicon nitride dielectrics. However, the long-term degradation pointed out by Liao would be expected to be problematic, and is consistent with the observation that the lifetime of switches made with silicon nitride dielectrics improves when they are hermetically sealed.

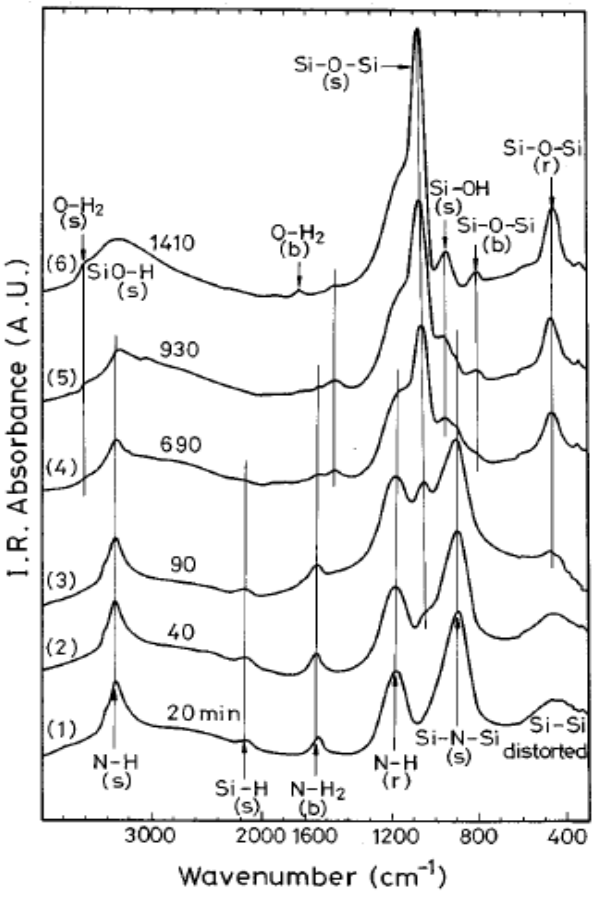

Figure 4.20 The IR spectra of PECVD a-SiN_x:H film deposited at 100 °C. Curves (1)-(6) indicate the IR spectra measured at different times after taking samples from reaction chamber.[15]

Stannowski *et al.*[16] studied the post-deposition oxidation in a-SiN_x:H films deposited by HWCVD (Hot-wire chemical vapor deposition) at temperatures in the range of 300-500°C. By using a FTIR (Fourier-transform infrared spectroscopy) technique,

they showed that stoichiometric (N/Si =1.33) silicon nitride and Si-rich (N/Si=0.8) silicon nitride weren't affected by air exposure for times up to 6 months (See Figure 4.21). In contrast, the N-rich silicon nitride samples revealed changes in the FTIR spectrum due to post-deposition oxidation for both short time and a long time exposures (in Figure 4.21, R=60 and 120 are N-rich). These data suggest that the stability of capacitive MEMS switches to air/moisture related degradation should be improved for higher temperature deposition processes, especially in more Si– rich compositions.

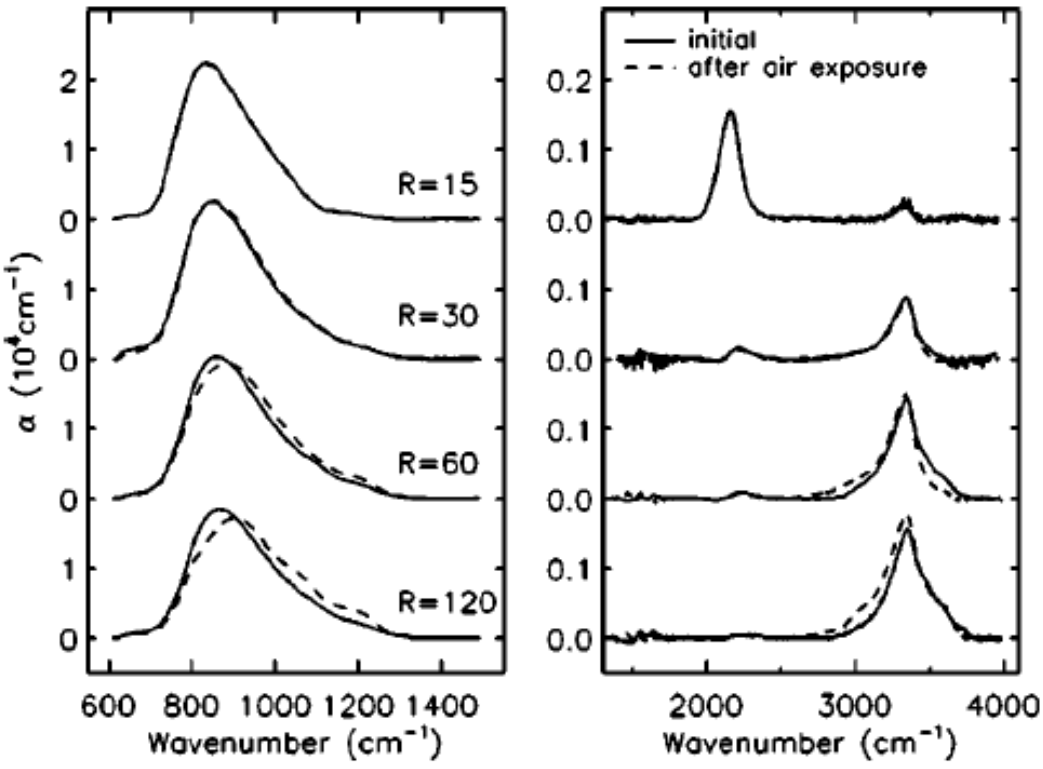

Figure 4.21 Infrared absorption spectra of a-SiN_x:H deposited with different gas flow rate ratios, measured after a few minutes and after six months of air exposure. α is the absorption coefficient. Curves are shifted vertically for clarity.[16]

4.6 Temperature Dependent Current-Voltage Response

To provide additional insight into the conduction mechanism in the silicon dielectric films, the current density at constant electric field was measured at different temperatures. Since both Poole-Frenkel and Schottky conduction mechanisms involve thermal promotion of carriers over some barrier (See Chapter 2), measurements as a function of temperature provide a way of determining the barrier height. Figure 4.22 shows the current density of the standard dielectric at different temperatures and electric fields. As described earlier, it was found that on the first heating, the current density for this dielectric decreases below its room temperature (298K) for temperatures between approximately 323K and 418K.

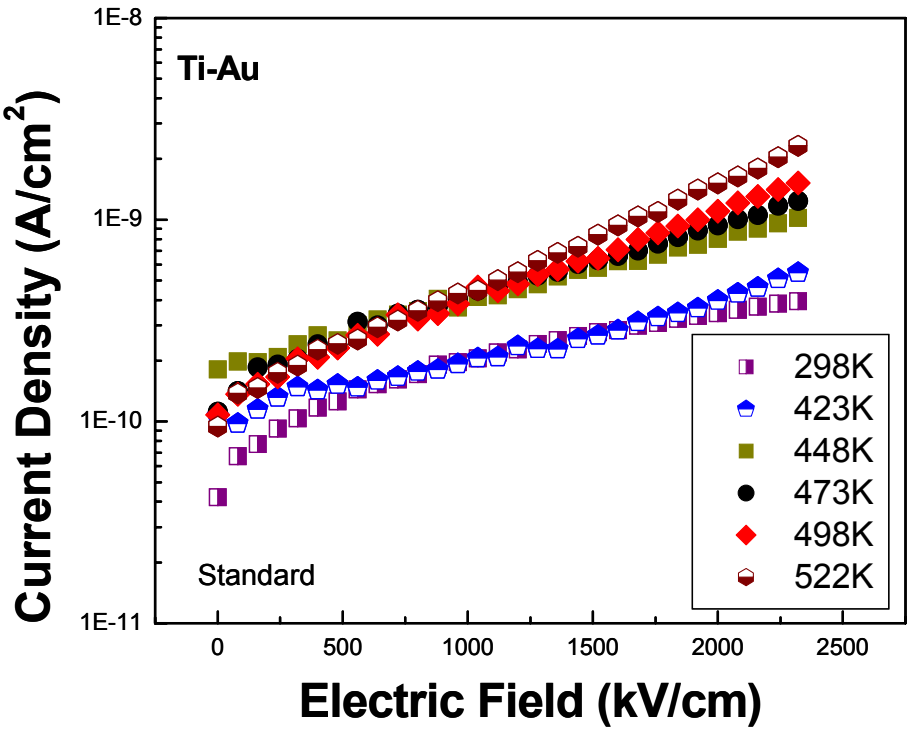

Figure 4.22 The plot of current density-electric field in the standard dielectric for different temperatures.

In order to verify whether the current density decrease was caused by electrode failure, the capacitor was cooled down to room temperature after each heat treatment and remeasured at the same field. It was found that heat treatment led to a reduction in the room temperature current as well (See Fig. 4.23). To minimize the impact of this on the determination of the barrier height, a capacitor was first heated to 473K. This is below the growth temperature, and it was hoped that this would not lead to large permanent changes in the film composition. As seen in Figure 4.24, the current density at room temperature decreases after heating the film for 10 minutes at 473K. The temperature dependence of the leakage current was then measured on heating. It has been reported that PECVD silicon nitride usually contains hydrogen in the range of 10-30at. %.[16] The evolution of hydrogen from CVD silicon nitride usually occurs above the deposition temperature and leads to an increase in tensile stress in the film due to the volumetric reduction.[17] Warren *et al.*[18] proposed that paramagnetic defect centers were formed due to the post-deposition annealing (>500^{o}C above deposition temperature) causing hydrogen evolution from the N-H site, leaving behind charged N^{-} ($^{-}N=Si_2$) and N^{+} ($^{+}N=Si_2$) dangling sites as paramagnetic trap centers in LPCVD and N-rich PECVD a-SiN_x:H. In this work, it is possible that the current density decrease at room temperature after heating the film at 473K may be due to partial elimination or redistribution of hydrogen.

The F dielectric was also soaked at constant temperatures from 298 K to 423 K so that the leakage current could be measured. Figures 4.25 (a-c) show the current density of the F dielectric measured at different temperatures and fields with different top electrodes. It can be seen that the current density increases with temperature for all measured electric fields with all top electrodes.

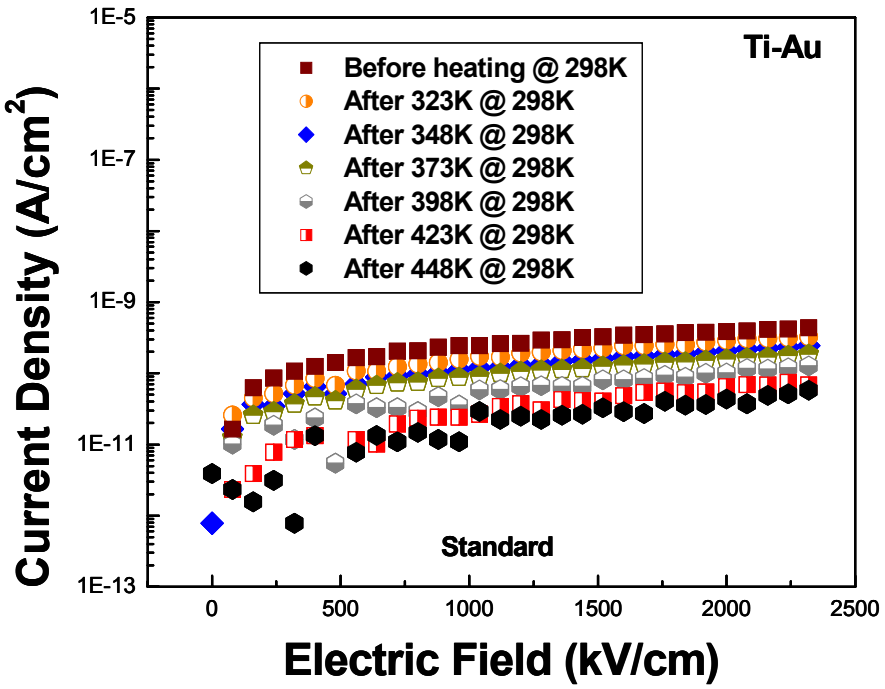

Figure 4.23 The plot of current density-electric field in the standard dielectric at 298K after heating to different temperatures.

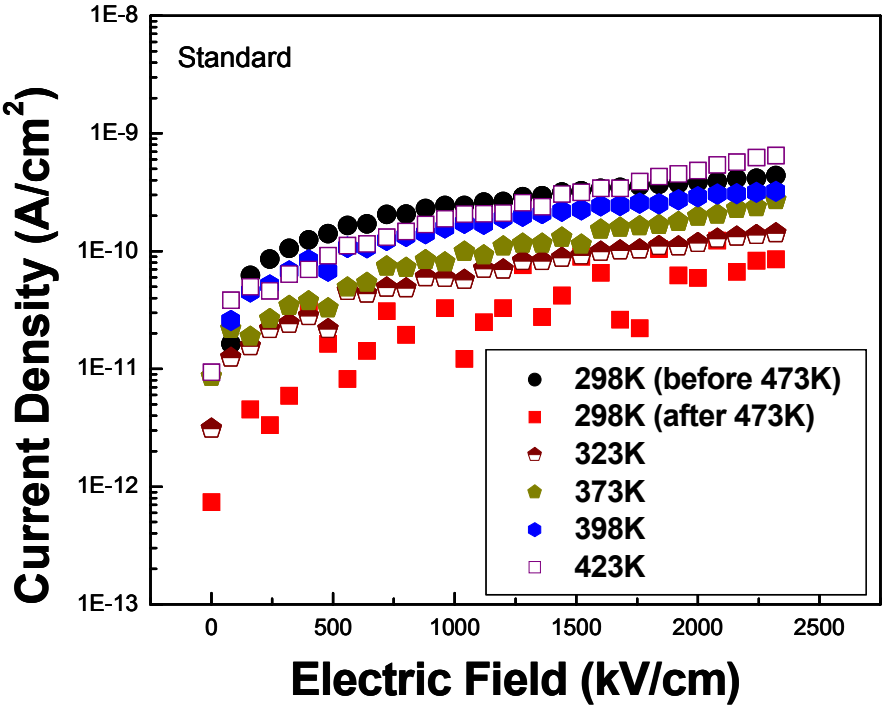

Figure 4.24 The current density as a function of the electric field measured for different temperatures after heating the film at 473K.

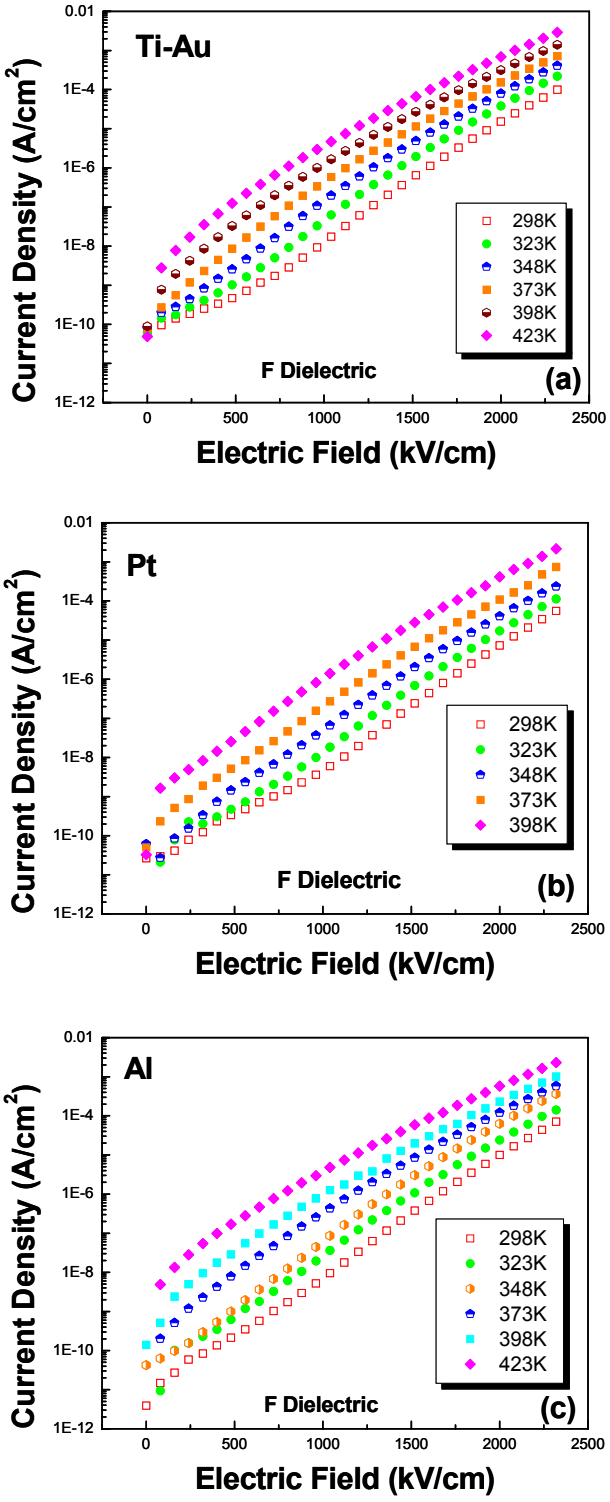

Figure 4.25 (a), (b), and (c) Current density-electric field response in the F dielectric for different temperatures with different metal electrodes.

4.7 Conduction Mechanisms in Silicon Nitride Dielectrics

In this section, the conduction mechanisms responsible for the current-voltage behavior of the two types of silicon nitride films were investigated. In particular, the electrode-limited Schottky mechanism, the bulk-limited Poole-Frenkel Mechanism and Fowler-Nordheim Tunneling were all considered.

4.7.1 Poole-Frenkel Mechanism

This bulk limited mechanism assumes that the trap barrier can be lowered with an applied external electric field, thus injecting the carriers into the conduction band of the insulator.[8] Ionization of the charge carriers into the conduction band of the insulator contributes to the current density as follows: [8,19]

$$\boldsymbol{J} = \boldsymbol{E} \times \sigma = \boldsymbol{E} \times \boldsymbol{C} \exp(-\frac{\boldsymbol{q}\Phi}{\boldsymbol{kT}}) \exp(\frac{\beta_{\boldsymbol{PF}} \sqrt{\boldsymbol{E}}}{\boldsymbol{kT}}) \qquad (4.5)$$

where *C, k, T, E, σ* are a pre-exponential factor, Boltzmann's constant, the absolute temperature, the electric field, and the electrical conductivity, respectively. Φ is the Poole-Frenkel barrier height and β_{PF} is Poole-Frenkel field lowering coefficient that is defined by:

$$\beta_{PF} = (\frac{q^3}{\pi \varepsilon_o \varepsilon_r})^{1/2} \qquad (4.6)$$

Using equation 4.5, the barrier lowering $(\Delta\phi)$ due to electric field is given by $\Delta\phi = (\frac{\beta_{PF} \boldsymbol{E}^{1/2}}{\boldsymbol{q}})$ for Poole-Frenkel emission. Notice that this barrier lowering is the same as Schottky lowering but without a factor of four in the denominator. Hence, one

can expect the barrier lowering for Schottky to be half that calculated for Poole-Frenkel dominated conduction ($\frac{1}{2}\beta_{PF} = \beta_s$).[8]

In order to determine if the conduction mechanism is controlled by the Poole-Frenkel mechanism (as has been reported previously for many silicon nitrides[22-24]), the dielectric constant can be calculated from the slope of *ln(J/E)* versus $E^{1/2}$ by fitting the data to equation 4.5. The obtained dielectric constant can be compared with the dielectric constant measured independently at optical frequencies. If the obtained dielectric constant from the linear fitting of the data is close to the dielectric constant measured independently at optical frequencies, it would mean that the dominant mechanism is controlled by Poole-Frenkel mechanism at these fields. [20]

Figure 4.26 shows the plots for the F dielectric. Only data at fields high enough that the true leakage regime was reached were used. The high frequency dielectric constant was computed to be 3.67±0.04, 3.28±0.06, and 3.4±0.03 using Ti-Au, Pt, and Al electrode, respectively. The optical dielectric constant for F dielectric was separately measured to be 4.4 at a wavelength of 630nm using spectroscopic ellipsometry (See Fig. 4.27).[2] The similarity in the electrically and optically determined high frequency dielectric constants strongly suggests that the conduction mechanism for the F dielectric is of the Poole-Frenkel type at electric fields above approximately 1MV/cm. This is also consistent with the observed lack of a top electrode dependence for the conductivity (See Fig. 4.15).

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[2] The spectroscopic ellipsometry data were collected and modeled by Tanawadee Dechakupt.

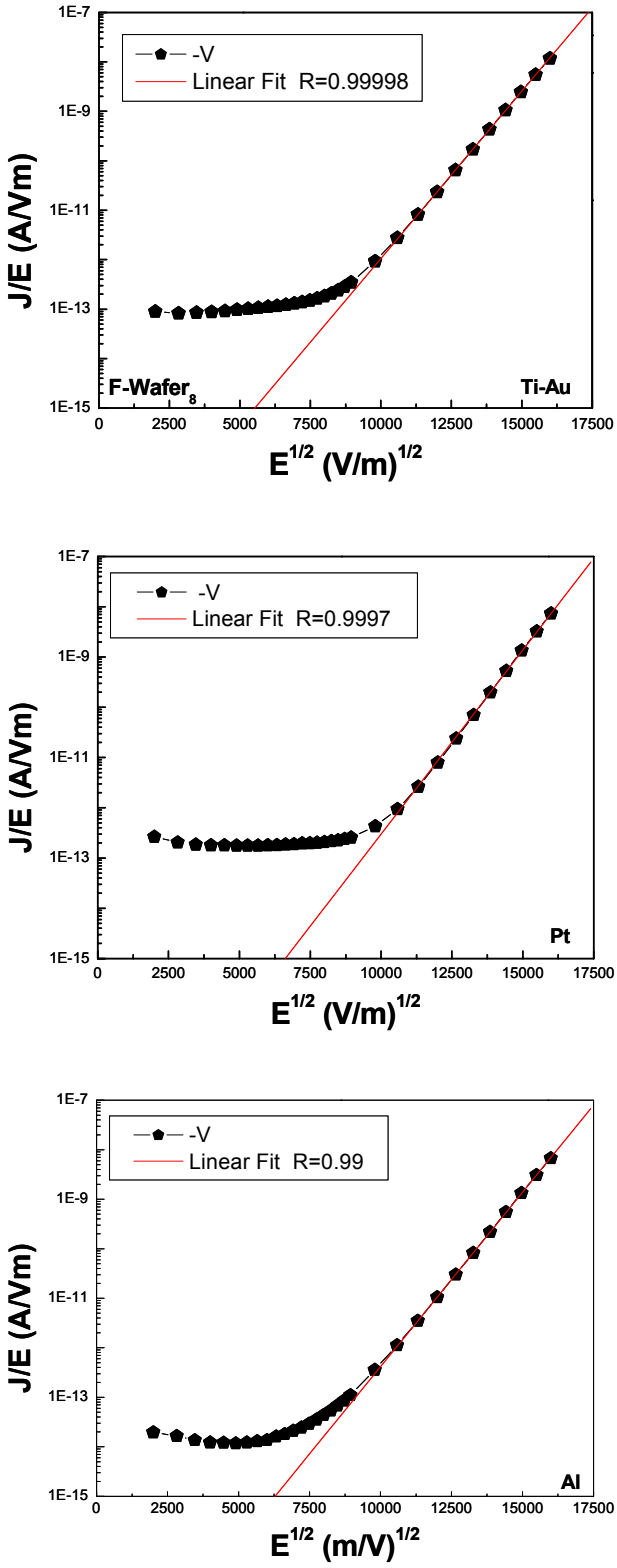

Figure 4.26 Dielectric constant estimation using Poole-Frenkel fitting with different metal electrodes for F dielectric.

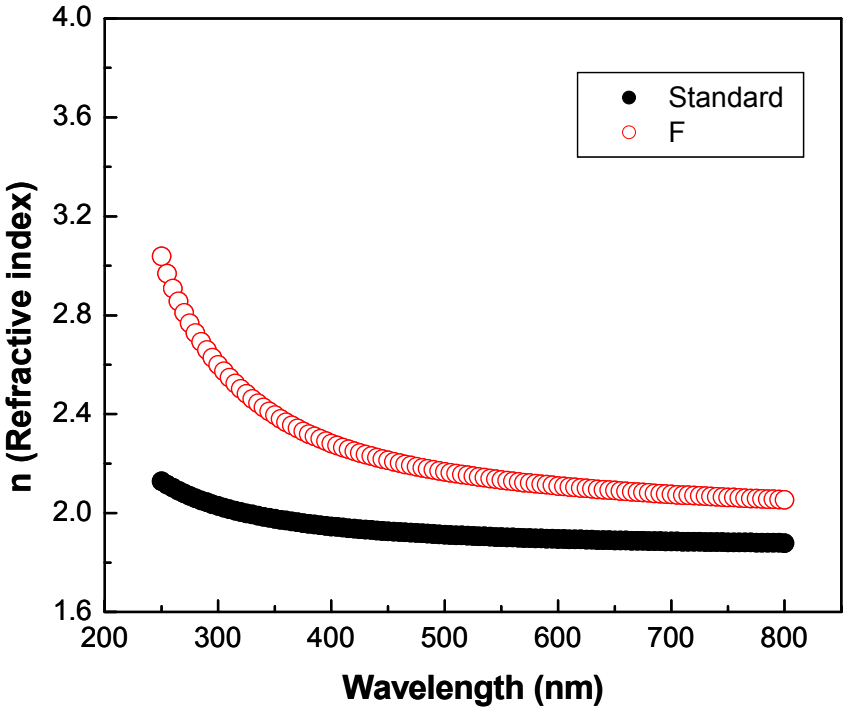

Figure 4.27 The refractive index as a function of the wavelength in the standard and F dielectric measured by ellipsometry.

A comparison of the optical property data of the F dielectric (n = 2.06) with that in Table 2.5 (See Table 2.5 in Chapter 2)[21] suggests that the F dielectric is indeed Si-rich and that the N/Si ratio is probably near N/Si =1.12. It can also be seen in Fig. 4.27 that the F dielectric shows substantially more dispersion than does the standard silicon nitride dielectric. This is also consistent with a lowering of the band gap and a low N/Si ratio.

Kaya *et al.*[22] studied Poole-Frenkel conduction in Si-rich PECVD silicon nitride films deposited at 250°C with flow rate ratios ($R=NH_3/SiH_4$) between 0.5 and 0.8. They calculated dynamic relative dielectric constants of films between 3 and 4. In addition, Hsieh *et al.*[23] reported dynamic relative dielectric constants between 3.52 and 4.10,

obtained from Poole-Frenkel slopes for the Si-rich PECVD a-SiN_x:H deposited at 300 ^oC. The current findings are in good agreement with the previous studies both in terms of conduction mechanism and the dynamic dielectric constant.

The leakage behavior as a function of temperature (measured at constant field = 2.32MV/cm) for the F dielectric was then used to determine the potential barrier height associated with the trap site. As seen in equation 4.5, a linear fit of *ln (J/E)* versus *(1/T)* gives a slope of

$$\boldsymbol{slope} = \left(\frac{-\boldsymbol{q}\phi_{\boldsymbol{B}} + \beta_{\boldsymbol{PF}}\boldsymbol{E}^{1/2}}{\boldsymbol{k}}\right) \qquad (4.7)$$

where (ϕ_B) is the charge trap barrier height known as the Poole-Frenkel barrier.[8] The results are shown in Figure 4.28. The barriers were found to be 0.84±0.01eV, 0.86±0.02eV, and 0.83±0.01eV for measurements made for Al, Pt, and Ti-Au top electrodes, respectively. As seen, the Poole-Frenkel barriers are independent of the electrode materials, as is expected for this conduction mechanism. The pre-exponential factors (C) for the F dielectric were estimated to be $2.52(\pm0.15)x10^{-4}$, $2.71(\pm0.16)x10^{-4}$, and $2.85(\pm0.25)x10^{-4}$ $AV^{-1}m^{-1}$ using Ti-Au, Al, and Pt electrode, respectively. Sze[24] reported this value to be 0.1 $AV^{-1}m^{-1}$ for LPCVD Si_3N_4 deposited at 1000^oC. Habermehl *et al*.[14] reported the pre-exponential factor to be $1.81x10^{-4}$ $AV^{-1}m^{-1}$ for $SiN_{1.22}$ and $2.75x10^{-4}$ $AV^{-1}m^{-1}$ for $SiN_{1.17}$ deposited by an LPCVD process at 800-850 ^oC. The differences were attributed to disparities in the carrier mobility and trap density in the nitrides.[14]

Kato *et al*.[25] reported the Poole-Frenkel barrier heights for several different compositions of silicon nitride films with N/Si ratios of 0.9 (open square in Figure 4.29),

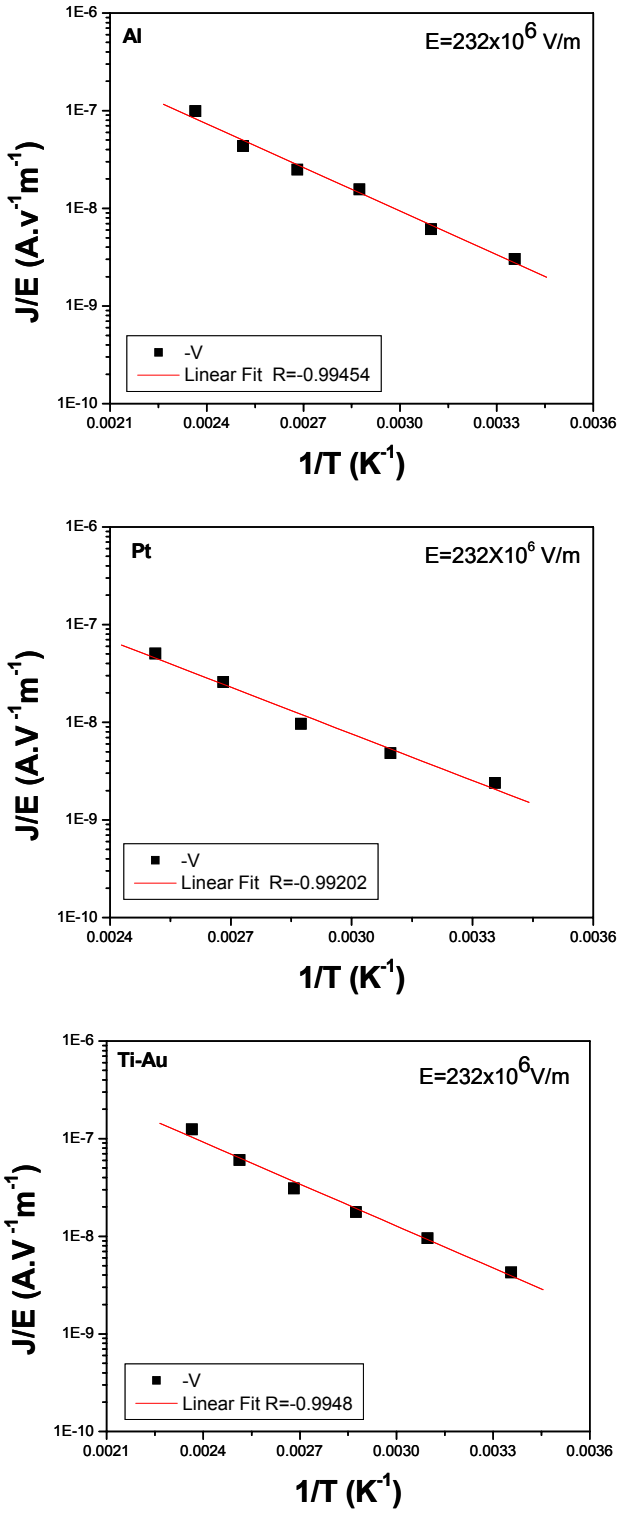

Figure 4.28 Linear fits for the estimation of Poole-Frenkel barriers using different electrodes in the F dielectric.

0.97 (open triangle), and 1.26 (open circle), respectively deposited by PECVD at 400 ^{o}C. The refractive indices for these films were 2.08, 1.99, and 1.91 at 632.8 nm. As depicted in Figure 4.29, the Poole-Frenkel potential barrier height increases with increasing N concentration in silicon nitride films. N/Si ratios of 0.9 and 0.97 provide Poole-Frenkel barrier heights approximately between 0.85 and 1eV.

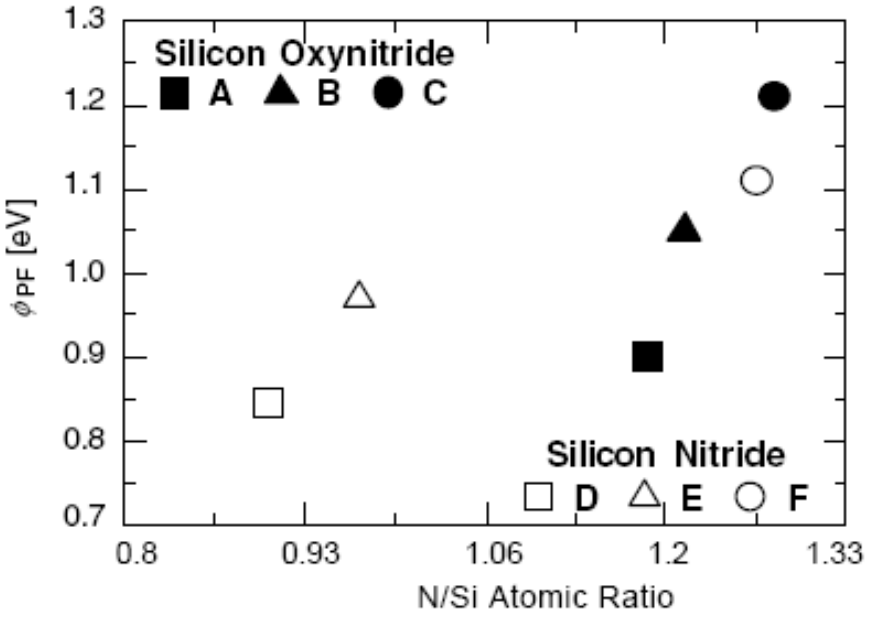

Figure 4.29 Poole-Frenkel barrier heights versus N/Si atomic ratios in the PECVD a-SiN_z:H and a-SiO_xN_y:H.[30]

Other authors have also shown that Poole-Frenkel potential barriers can be lowered by introducing more Si into silicon nitride films.[14] As depicted in Table 4.3, it was found that over a composition range from $SiN_{1.33}$ to $SiN_{0.54}$ the Poole-Frenkel barrier height was reduced from 1.08 to 0.55eV, and the residual Si-N bond strain was decreased from 0.006 to -0.0026. The reduction in bond strain was structurally related to a volumetric distortion in the Si centered tetrahedra as Si was substituted for N. This

resulted in a reduction in the barrier height for Poole-Frenkel trap emission. A comparison of the pre-exponential term and barrier heights of the F dielectric with the data in Table 4.3 also suggest a composition between N:Si of 1.1 and 1.2.

Table 4.3 The estimated Poole-Frenkel barrier heights in silicon nitride films of different composition.[14]

Composition	C_1 ($A\,V^{-1}\,m^{-1}$)	Φ_B (eV)	Residual strain, ε_r
$SiN_{1.33}$	$1.44\ (\pm 0.08)\times 10^{-5}$	1.08 ± 0.05	6.0×10^{-3}
$SiN_{1.22}$	$1.81\ (\pm 0.15)\times 10^{-4}$	0.91 ± 0.01	2.0×10^{-3}
$SiN_{1.17}$	$2.75\ (\pm 0.50)\times 10^{-3}$	0.69 ± 0.05	8.0×10^{-5}
$SiN_{0.78}$	$1.38\ (\pm 0.28)\times 10^{-2}$	0.44 ± 0.01	-2.0×10^{-3}
$SiN_{0.54}$	3.86 ± 0.16	0.55 ± 0.02	-2.6×10^{-3}

It is important to note that the reduction in Poole-Frenkel barrier height may have an important impact on the reliability of capacitive MEMS switches made with silicon nitride. To avoid difficulties associated with stiction of the bridge due to trapped charges, it is important either to make it difficult to inject charges in the first place, or easier to detrap charges once they are injected. The modest dependence of the current density on electrode in the F dielectrics suggests that it will not be possible to engineer the injection through changes in the electrode. Consequently, it is expected that the lowering of the trap barrier height will increase the lifetime of capacitive MEMS switches by enabling trapped charges to be removed from the film more readily. It is also important to note, however, that a barrier height of ~0.8 eV is still substantial at room temperature. It is likely that further increases in the reliability of capacitive MEMS switches would be obtained if alternative dielectrics with smaller barrier heights were explored.

Capacitive switches were also used for the I-V characterization of the silicon nitride films in order to demonstrate whether the data for capacitive switches and MIM capacitors are consistent with each other. Measurements were made either by applying a high enough voltage to pull the bridge into contact electrostatically, or by measuring bridges that were already stuck down. In Figure 4.30, the current density–field data for a capacitive switch with an F dielectric was compared to MIM capacitors with different top

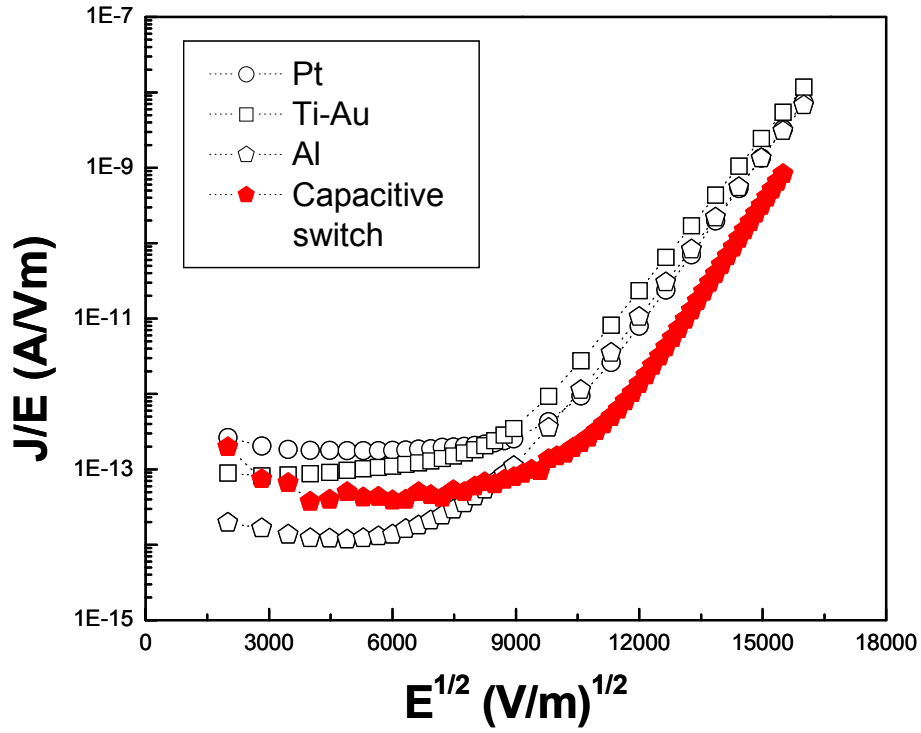

Figure 4.30 Poole-Frenkel comparison of different metal electrodes with a capacitive switch.

metal electrodes. As can be seen, the shapes of the curves are quite similar, suggesting that the MIM structure is a reasonable way to investigate conduction mechanisms in the switch. Additionally, Figure 4.31 shows the dielectric constant estimation of the F dielectric using capacitive switches with a Ti-Au bridge for the experiment. The

dielectric constant was estimated to be 2.84±0.07. This value is somewhat lower than that for the MIM capacitors, but is still suggestive that the Poole-Frenkel mechanism is operating in the switch dielectric at high fields (>1MV.cm^{-1}). This reiterates the importance of the Poole-Frenkel barrier height in controlling the switch reliability.

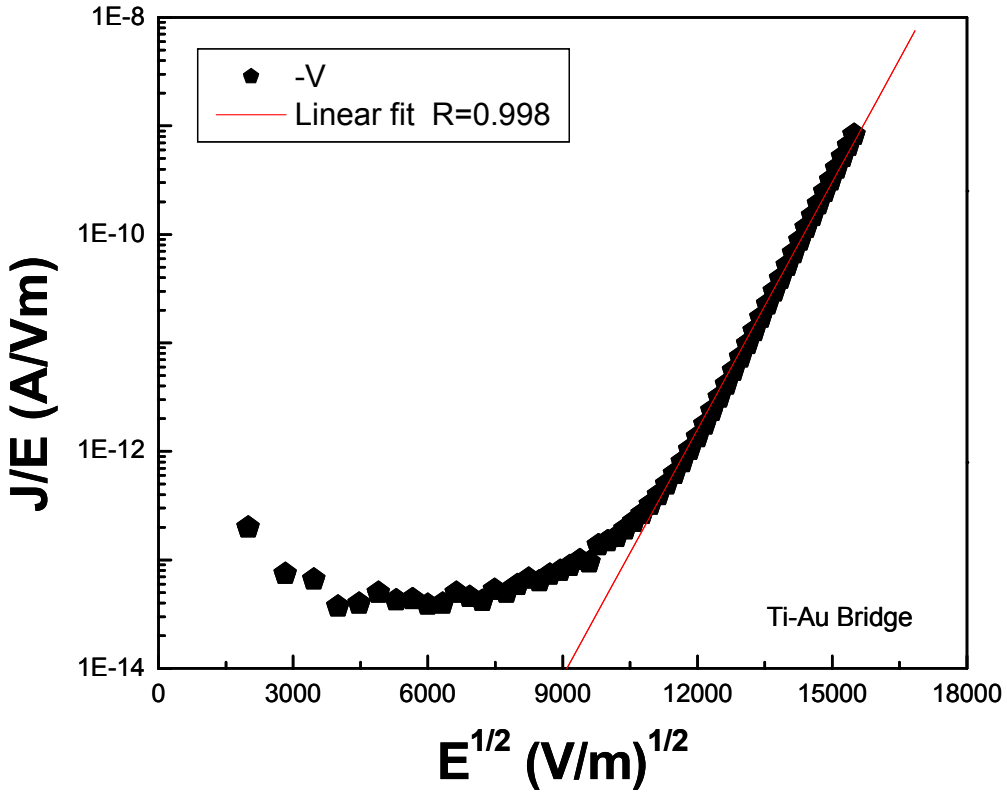

Figure 4.31 Linear fit to the Poole-Frenkel mechanism measured on a capacitive switch with a Ti-Au bridge.

4.7.2 Richardson-Schottky Mechanism

In the standard dielectric at all measured fields, and the F dielectric at lower electric fields, the current density was observed to be a function of the electrode utilized, suggesting that an interfacial barrier might be controlling the conduction. When the

transport of charges between an electrode and insulator is limited by the barrier between them, the current depends on the number of charge carriers that can overcome the barrier.[26] Hence, thermal excitation of the charge carriers over the interfacial barrier increases the current density in the insulator. The combination of Richardson thermoionic emission and barrier lowering due to the Schottky effect is given by the Richardson-Schottky equation [8] (Schottky 1914):

$$J = AT^2 \exp(-\frac{q\phi}{kT}) \exp(\frac{\beta_S E^{1/2}}{kT}) \qquad (4.8)$$

where A is the effective Richardson constant, which incorporates the carrier mobility, ϕ is the interfacial barrier height, q is the carrier charge, T is temperature, E is electric field, k is Boltzmann's constant, and β_s is the field lowering coefficient which is given by

$$\beta_s = (\frac{q^3}{4\pi \varepsilon_r \varepsilon_o})^{1/2} \qquad (4.9)$$

where ε_r is the high frequency dielectric constant and ε_o is the free space permittivity. Using equation 4.8, $(\frac{\beta_s \boldsymbol{E}^{1/2}}{\boldsymbol{q}})$ is the barrier lowering $(\Delta\phi)$ due to the Schottky effect caused by the applied electric field.

The field dependence of the conductivity is the same for the Schottky and the Poole-Frenkel mechanisms.[20] Fortunately, these mechanisms can be distinguished relatively easily by fitting the data to both mechanisms over the same field region. Then, the estimated dynamic dielectric constant for both mechanisms can be compared with the high frequency dielectric constant for the material.[20] One of these mechanisms should provide a suitable dielectric constant, confirming the mechanism governing the

conduction.[20,27] For example, Maeda *et al.*[27] studied the conduction mechanisms in PECVD silicon nitride with different compositions (from Si-rich to N-rich) deposited between 250°C and 350°C. They estimated dielectric constants from the data at fields up to 1MV/cm. In addition, they independently measured the optical dielectric constants for their films. Table 4.4 summarizes the results. As seen in the Table, the dynamic dielectric constants received for Poole-Frenkel slopes agree with the optical values. Conversely, the dielectric constants estimated from the Schottky slopes are too small to be credible.

Table 4.4 The estimated dielectric constants from linear fitted data to the Poole-Frenkel and Schottky mechanism.[27]

Sample no.	ϵ_d ($\pm$ 0.02)[a]		ϵ_s ($\pm$ 0.1)[b]	ϵ_0 ($\pm$ 0.03)[c]
	Poole-Frenkel	Schottky		
1	3.89	0.97	7.56	3.88
2	3.87	0.97	6.86	3.88
3	3.88	0.97	6.31	3.92
4	4.15	1.04	6.52	4.12
5	4.36	1.09	6.87	4.20

[a] Dynamic dielectric constant.
[b] Static dielectric constant.
[c] Optical dielectric constant.

By using the same electric field regions where the Poole-Frenkel dynamic dielectric constant was obtained, the dynamic dielectric constant was estimated for the F dielectric from slope of lnJ versus $E^{1/2}$ by fitting the data to the Schottky equation. Figure 4.32 shows the Schottky plot of the F dielectric used to estimate the dynamic dielectric constant. The obtained dielectric constant was found to be 0.753±0.005, which is

unphysical. This indicates that the conduction mechanism in these field regions isn't Schottky type.

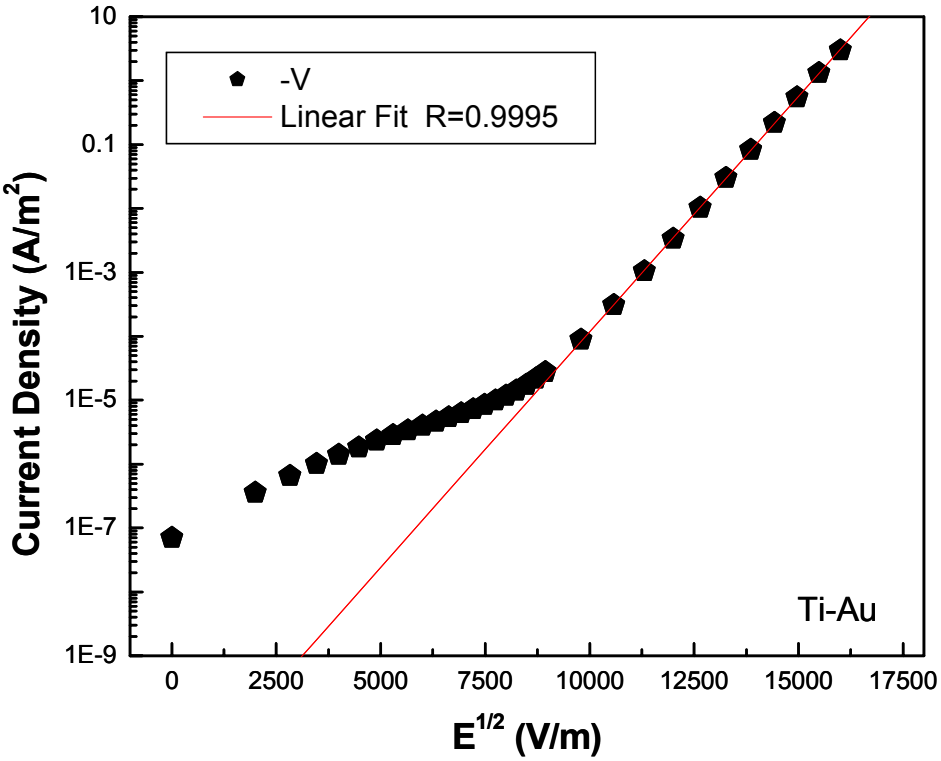

Figure 4.32 The dielectric constant estimation from the linear fitted data to the Schottky equation for the F dielectric.

In addition, Schottky emission is an electrode controlled mechanism, and thus the current density of the system should change with the work function of the electrodes.[2,8] Figure 4.33 shows the current density of the F dielectric measured using different electrodes. It is clear that at high field regions the current density doesn't change with electrodes. Therefore, it was concluded that in the F dielectric where true leakage currents could be measured, the dominant conduction mechanism is Poole-Frenkel. Further work should be done to investigate why the polarization currents in both standard

and F nitrides were electrode dependent (See Fig. 4.14 and 4.33).

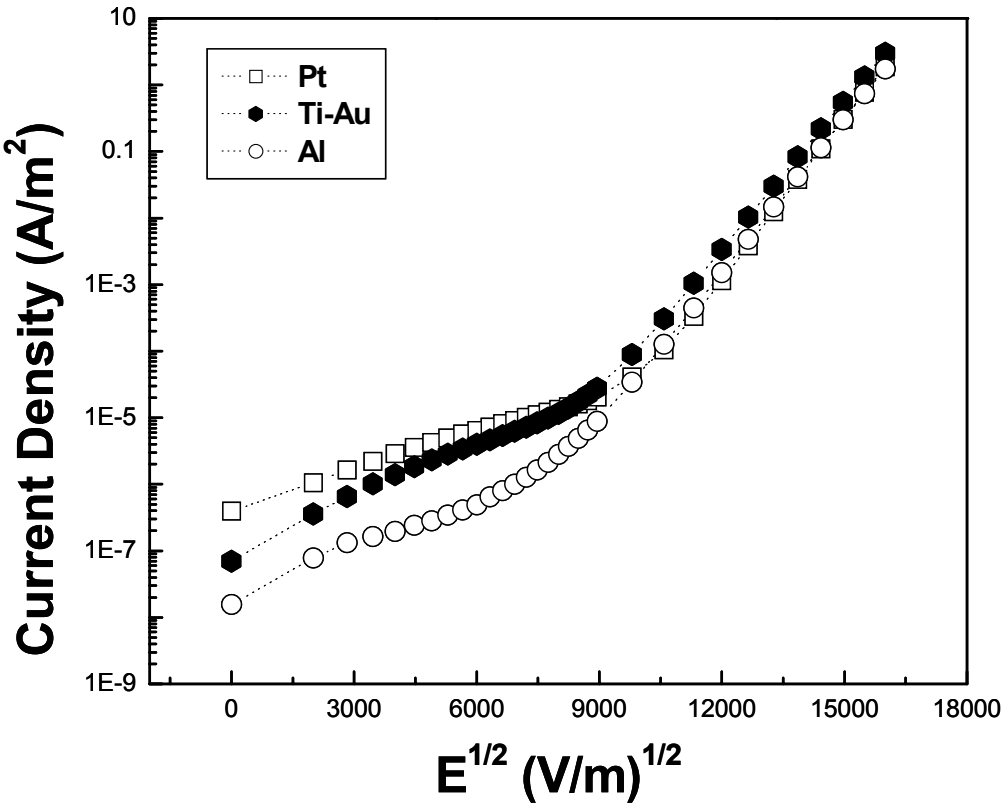

Figure 4.33 Schottky Plots of the F dielectric using different metal electrodes.

4.7.3 Fowler-Nordheim Tunneling

It is also possible, in principle, for field-assisted tunneling of the electron through a potential barrier into the conduction band of the insulator to dominate conduction. This effect can be observed at higher fields due to the thinning of a triangular barrier that allows carrier injection from the Fermi level of the metal into the conduction band of the insulator.[28]

Fowler-Nordheim tunneling was reported to occur in very thin silicon nitride films.[28,29] The current density due to tunneling is given by: [28]

$$J_{FN} = \frac{q^2 E^2}{16\pi^2 \frac{m^*}{m} \hbar \Phi_B} \exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E} \right] \qquad (4.10)$$

where m is the mass of an electron in free space, m^* is the effective mass of an electron in the crystal ($m \approx 0.4m^*$), $\hbar$ is Planck's constant/2π, and Φ_B is the barrier height for tunneling. It can be seen that this equation does not entail any thermal activation, and yields a temperature independent current density.

Bosa *et al.*[28] studied silicon nitride films deposited at 250°C by PECVD with thicknesses in the range of 394Å to 578 Å. They reported Fowler-Nordheim tunneling for their N-rich (N/Si=1.63) and nearly stoichiometric silicon nitride films at high fields (0.8MV/cm). However, they didn't observe tunneling for the Si-rich composition (N/Si=0.96) and believed that Poole-Frenkel conduction dominated for this composition.

The temperature dependent study can distinguish Poole-Frenkel conduction from Fowler-Nordheim tunneling. As mentioned earlier, the Poole-Frenkel mechanism is a thermally activated process, but Fowler-Nordheim tunneling is temperature independent.[25] Thus, the current density of the F dielectric was compared at different temperatures.

As shown in Figure 4.25, for the field range investigated in this study, the current density was temperature dependent. Consequently, there is no clear region where Fowler-Nordheim tunneling dominates the observed conduction, which is reasonable for these thick films. There is some indication that there is slightly lower temperature dependence at the highest fields. Consequently, it is possible that tunneling would become more important at electric fields beyond those used in this study.

4.8 Thickness Dependence of Current – Voltage Response

The conduction behavior was also studied using different film thicknesses. As observed earlier, at higher fields, the F dielectric showed Poole-Frenkel behavior, which can be attributed to the bulk properties of the film, which should not be strongly thickness dependent.[24] Figure 4.34 shows the F dielectric films with different thicknesses plotted using the Poole-Frenkel mechanism. As seen there, little thickness dependence is observed for films between 1600Å and 4000Å thick. It is not clear whether the small difference for the 1600Å film is statistically significant

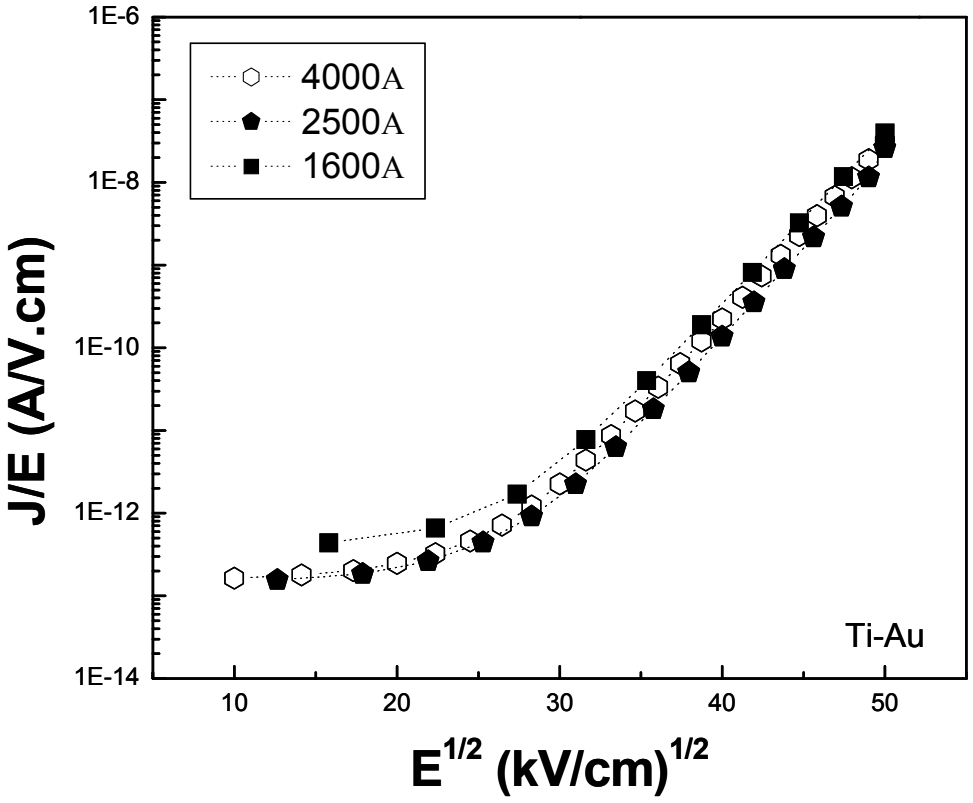

Figure 4.34 Thickness dependence of the Poole-Frenkel conduction in the F silicon nitride films.

Watanabe *et al.*[30] studied a low pressure N-rich silicon nitride (N/Si=1.5) deposited at 780°C and observed the current density changes as a function of the applied field for films less than 600Å thick. The biggest differences were observed for the thinnest films. As seen in Figure 4.35, the films with thicknesses of 300-500Å showed higher current densities than those of thicker films (1000-1500 Å). In addition, there is a slight difference between thicker films at high fields. They proposed that the electric field in the film and at the interface changes with thickness due to the formation of a space charge region located less than 600Å thick.

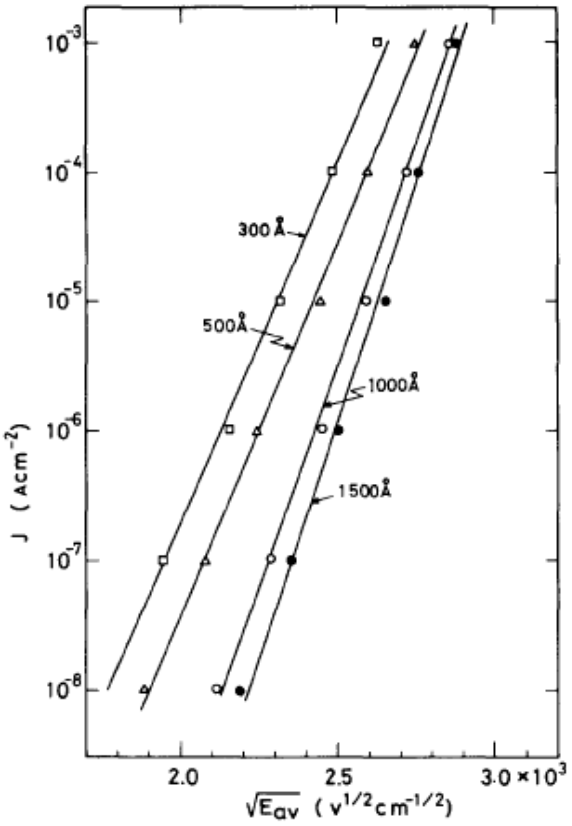

Figure 4.35 Current density as function of the electric field for different film thicknesses.[30]

4.9 The Effect of Switching Polarity on the Standard Silicon Nitride Dielectric

In this section, the short term and long term recovery of charges was investigated in the silicon nitride films. I) Short term behavior was probed by repeatedly measuring the current-voltage response for different polarities. This behavior was studied at low fields to monitor the recovery of transient currents as a function of the time. II) Additionally, the dielectrics were stressed under electric fields for a long time (23-24 hours) to observe the permanent changes that might affect the conduction behavior of the silicon nitride, and thus the device failures caused by stiction.

4.9.1 Short Term Recovery in the Standard Dielectric

The effect of electric field stresses as well as discharging time intervals on the current density was studied for the standard dielectric. Of interest was whether stressing of the standard dielectric changed the relaxation behavior of films and the measured current density.

It was suggested by Dietz *et al*.,[2] who studied the leakage current behavior of $SrTiO_3$ thin films prepared by an MOD process, that charging the dielectric may well take a longer time than its discharging. Hence, sufficient time should be given to charge and discharge the capacitor in order to reach the desired states.[2,6,26] Since polarization and depolarization currents are identical, but have opposite sign, it is hard to distinguish them from one another when the voltage polarity is reversed partially through a discharge cycle.[2,6,26]

As depicted in Figure 4.36, a measurement of the leakage current was carried out using a voltage staircase mode for each polarity. Subsequently, the voltage polarity was

reversed, and the staircase measurement was repeated. The polarity was then switched back to the original one, and the leakage measured a third time. In the figure, the numbers "1", "2", and "3" refer to the order in which the voltages were applied and (+) and (-) refer to the sign of the voltage applied to the bottom electrode used in the measurement.

As seen in Figure 4.36, the low field current densities are higher than their initial values when measured shortly after the polarity is switched. This was true whether or not the sample was first exposed to positive or negative polarities.

In order to determine whether or not the polarity change or simply the exposure to high fields was responsible for the observed increased current density, a measurement was carried out with no polarity change between voltage sweeps.

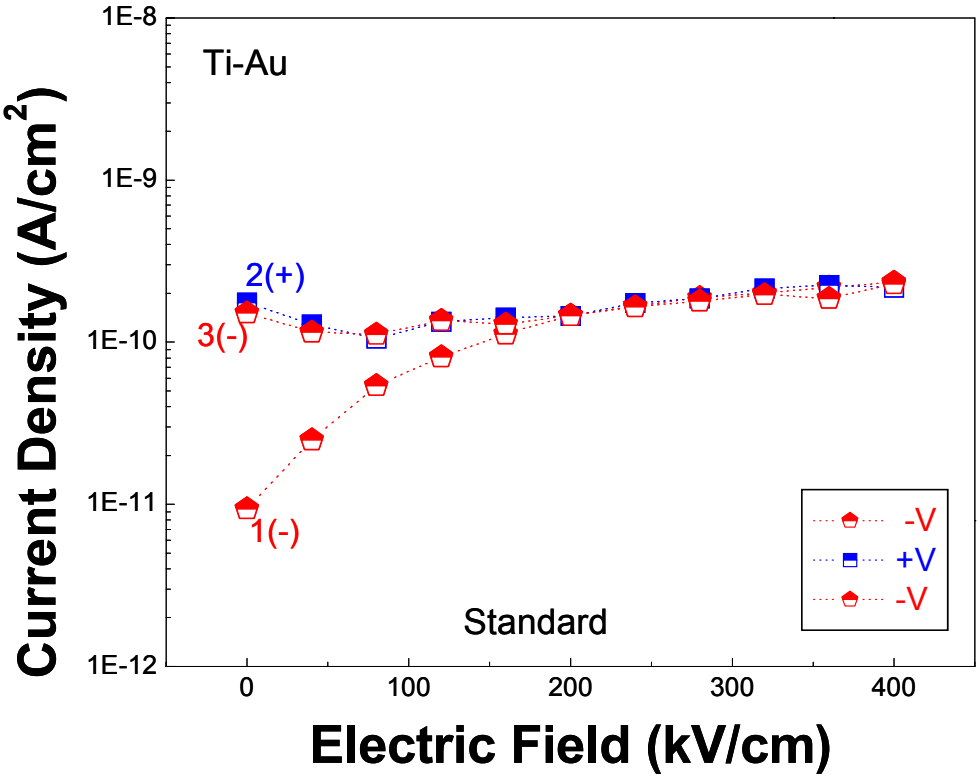

Figure 4.36 Repeated polarity changes at lower fields (<410kV/cm) with no long time delay between measurements.

As shown in Figure 4.37, this led to a substantial decrease in the low field current density. In addition, some currents for second and third sweeps have the "wrong" polarity, i.e. they are opposite in sign to the charging currents and thus these currents don't appear on a log scale plot (see Figure 4.38).

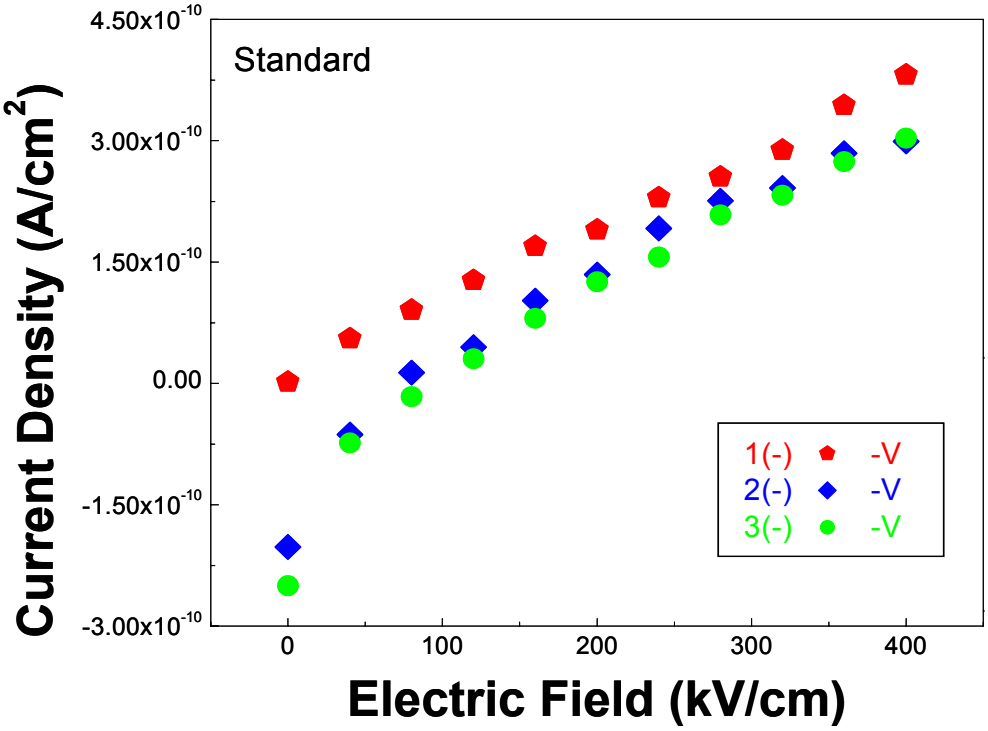

Figure 4.37 Current density measured three times at the same polarity.

There are a couple of possible mechanisms, which could be responsible for the increase in the current density after polarity change. First, it is possible that the measured leakage currents are the sum of the polarization currents on charging and the depolarization currents from the prior field stress. This would yield an increased low field current density for time scales, which correspond to the depolarization. Secondly, it is possible that injection of charges at the metal-dielectric interface at high voltage

stresses change the barrier heights for subsequent injection.[31] Interfacial barrier heights are believed to be important here since the standard silicon nitride dielectrics showed a dependence of the current density on top electrode type (See Fig. 4.14).

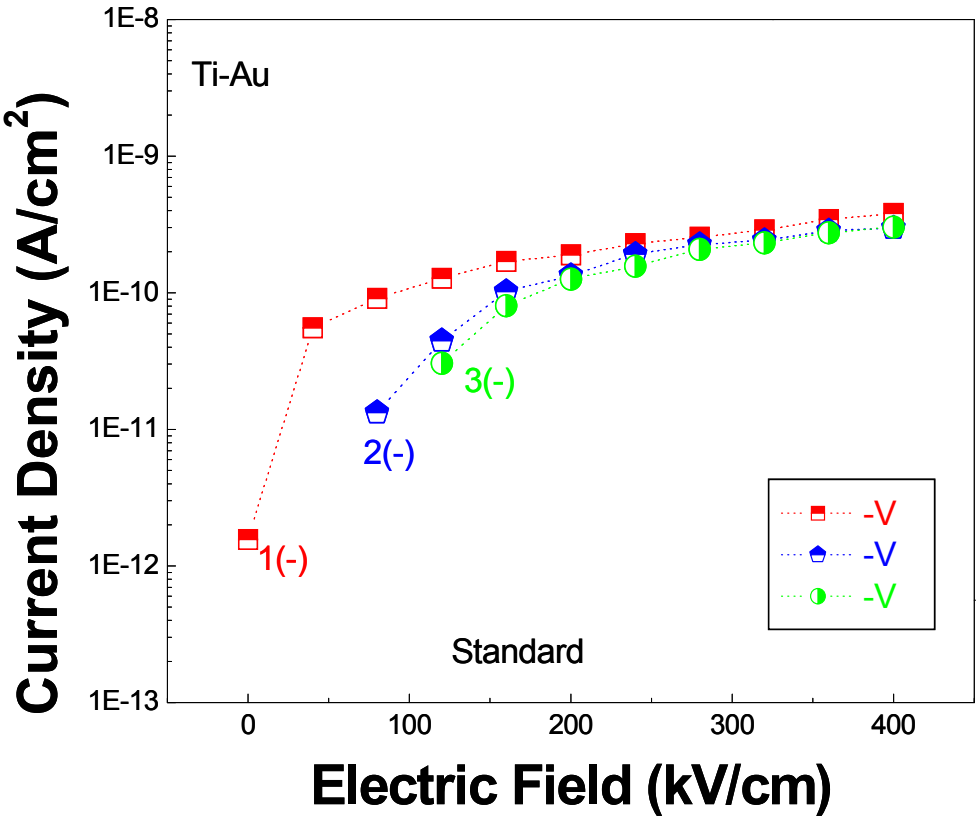

Figure 4.38 Low field current densities measured for three subsequent applications of field (64 second holding time at each voltage).

Depending on the injected carrier type, these charges increase or decrease the barrier at the interface, thus affecting the rate of carrier injection over the barrier. At the interface, this barrier lowering ($\Delta\Phi$) due to the image force (the attraction of negative and positive charges) is given by [6,8]

$$\Delta\Phi = \sqrt{\frac{qE}{4\pi\varepsilon}} \qquad (4.11)$$

where E indicates the field at the barrier as the source for barrier lowering and ε is the dielectric constant of the barrier region. Furthermore, when the polarity is switched, the interface remains charged and attracts more charge to be injected, consequently increasing the current density in the insulator.[31] When injection occurs with no polarity change, charges from the prior injection reduce new injection events due to the repulsion force that build up, thus causing the barrier to increase at interface.[20,31] In this case, the barrier change calculated from equation 4.11 should be added to the barrier at the interface.[2,8]

Furthermore, Figure 4.39 (a-b) shows that the observed increase in low field

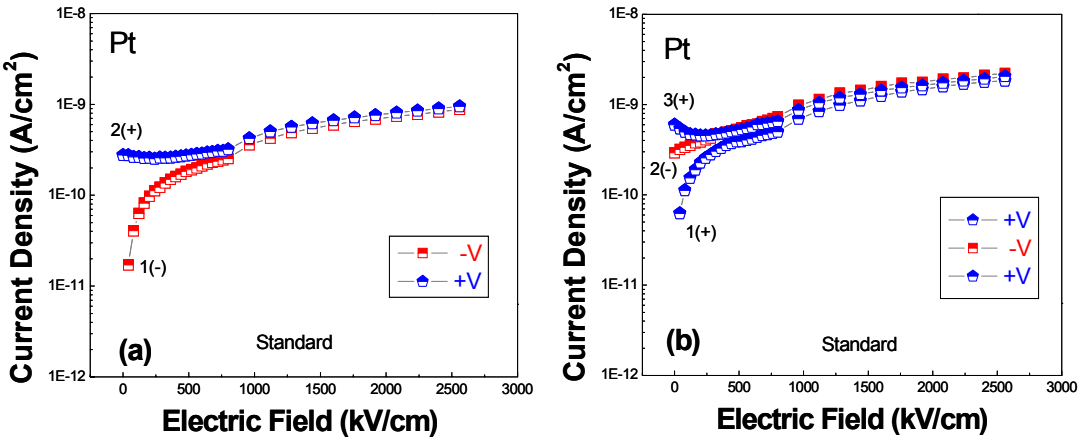

Figure 4.39 (a) Applied negative polarity was switched to positive polarity after a long stress (negative polarity first) **(b)** Applied positive polarity was switched to negative polarity and then switched back to positive polarity (positive polarity first).

measurement was made with a 64 second holding time and a maximum field of 2560 $kV.cm^{-1}$. Again, it is clear that increased current density does not depend on the initial polarity. In addition, it was found that the increase was most notable when the sample had been exposed to high fields for long times.

Figure 4.40 shows the current voltage response of standard dielectrics at different time intervals after stressing. The dielectric was initially stressed with an electric field of 600kV.cm^{-1} using Ti-Au electrodes for 6.4 minutes. The same electrodes were then measured at opposite polarity at different time intervals from 1 minute to 30 minutes at the electric field of 600kV.cm^{-1}. As seen in Figure 4.40, the shape of the current density curve recovers in less than 1 hour. The comparatively long recovery times could be problematic in a switch.

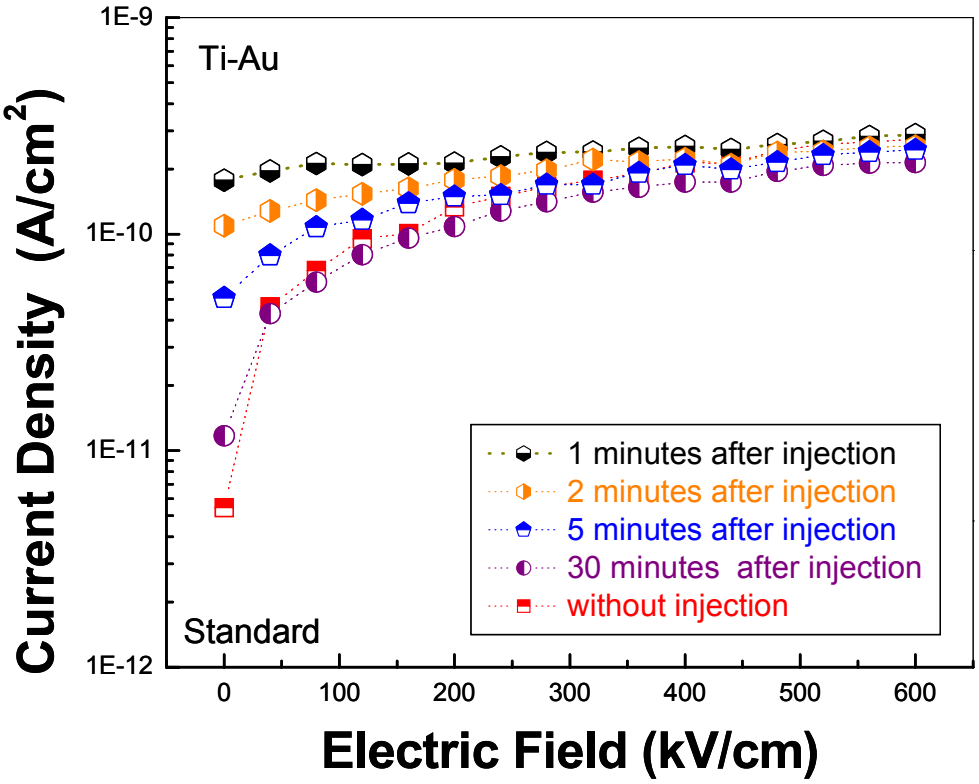

Figure 4.40 Recovery of charges for short time frames at lower fields (≤600kV.cm^{-1}).

4.9.2 Long Term Charge Recovery and Stressing of Silicon Nitride Dielectrics

The recovery of the silicon nitride to its initial state was studied by making current voltage measurements at different time intervals after stressing the capacitor structures. Figures 4.41 (a-b) show the recovery of the stressed capacitors with time for both the standard and F dielectric. The dielectrics were first stressed with a positive electric field of 400kV.cm^{-1} for 1 minute to 30 minutes. Subsequently, the currents were measured at negative polarity at a maximum electric field of 400kV.cm^{-1} immediately after stressing. Additionally, the recoveries of these charges were measured at the negative polarities after 1 day of holding the sample under open circuit conditions. For these stressing conditions, it was found that the charges recovered within 1 day and there was no permanent change in the dielectrics.

However, it is also important to examine how the dielectric behaves after much longer exposures to field (as for example might be experienced by switches as the cumulative time spent under field). As shown in Figure 4.42, the standard dielectric was stressed under an electric field of 4000kV.cm^{-1} for 23 hours. The current density of the dielectric was measured using the same electrode 1 day later. As seen in Figure, the current density is higher that the one measured prior to the electric field stress. This result indicates that standard dielectric shows a permanent change after the higher field stress for a long time. This permanent degradation might be due to a change in the interface states (perhaps a barrier height change) or to some other form of resistance degradation. Again, these currents are polarization currents, and there is no indication from the shape of the curve for a change in the conduction mechanism caused by stressing.

As shown in Figure 4.43, the F dielectric was stressed at an electric field of 2600

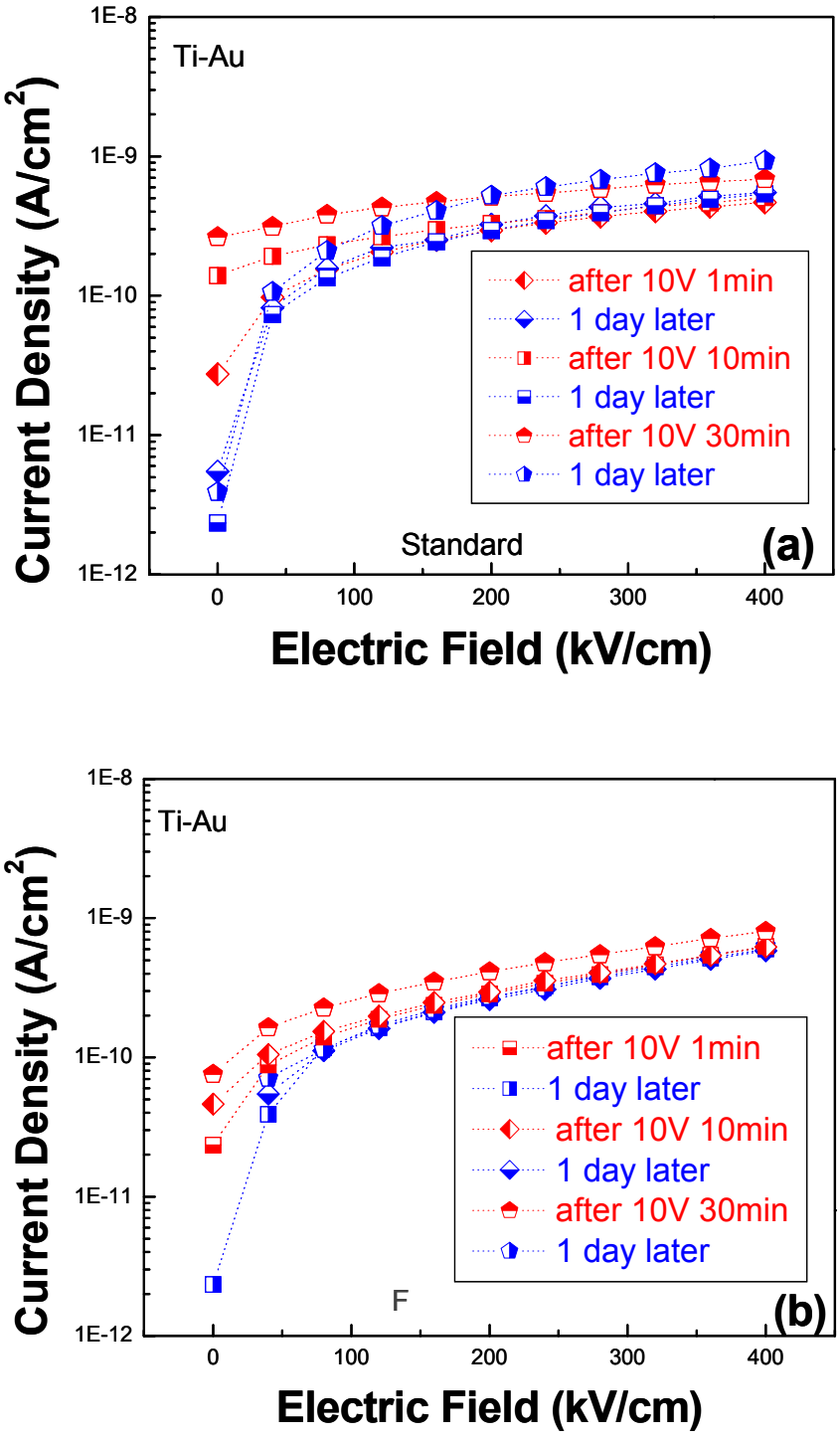

Figure 4.41 **(a)** The recovery of the charges after 1 day in the standard dielectric at lower fields (≤400kV.cm^{-1}). **(b)** The recovery of the charges after 1 day in F dielectric at lower fields (≤400kV.cm^{-1}).

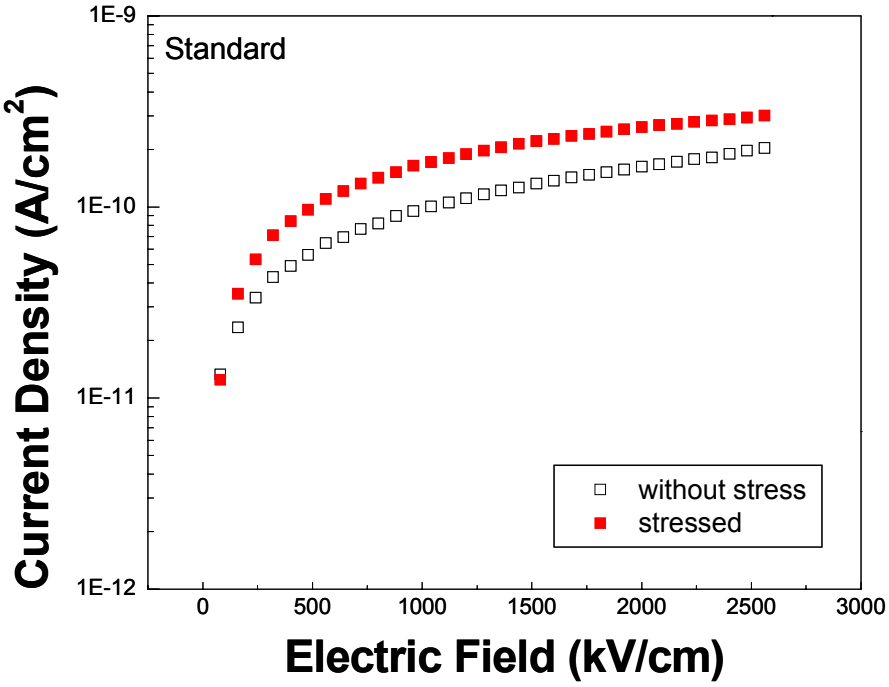

Figure 4.42 The long term electric field stressing of the standard dielectric.

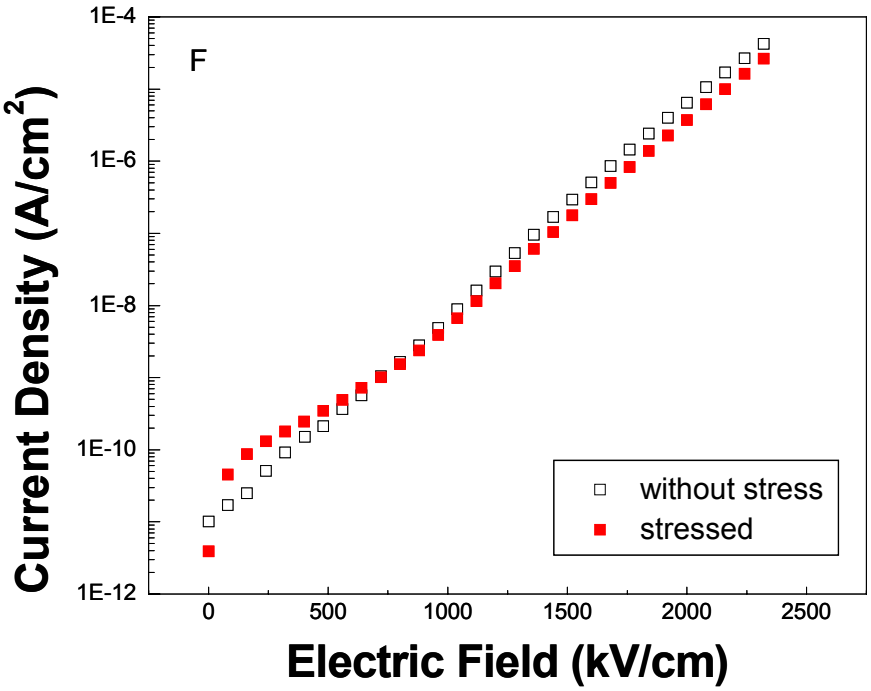

Figure 4.43 The long term electric field stressing of the F dielectric.

$kV.cm^{-1}$ for 24 hours. The current density was then measured 1 day later. As can be seen, there is only a slight change in the current density either at low fields (<1000$kV.cm^{-1}$) or high fields for this dielectric. Thus, the F dielectric was likely less affected by a long term electric field stress than the standard dielectric. This is true despite the fact that a considerably larger amount of charge passed through the F dielectric during the stressing, due to its higher conductivity at high fields.

4.10 Characterization of Silicon Nitride Films Using AC Signals

The response of silicon nitride dielectrics to ac electric fields was studied over a frequency range of 150mHz -100 kHz in order to investigate the possibility of interfacial polarization and its relation to charge trapping. AC signals can be used to provide a comprehensive understanding of the electrode-dielectric interface and/or barriers between dissimilar phases with different conductivities.[32] When an ac sinusoidal potential ($V=V_o.e^{i\omega t}$) is applied to a dielectric, the net response consists of a charging current and a loss current that are related to the dielectric constant.[33] The complex dielectric constant in a dielectric can be written as [34]

$$\varepsilon^* = \varepsilon' - \boldsymbol{j}\varepsilon'' \qquad (4.12)$$

where the complex dielectric constant (ε^*) is made up of a real part (ε') that describes charge storage and an imaginary part (ε'') that represents the loss in the dielectric medium. The loss factor $(\tan\delta)$ is given by the ratio of the imaginary part (the energy lost) to the real part (the energy stored): [34]

$$\tan\delta = \varepsilon'' / \varepsilon' \qquad (4.13)$$

In this work, it was interesting to determine if ac measurements could be used to identify a discrete layer in the film whose properties had been changed by injected charge. In such a case, the effective dielectric relaxation mechanism can be explained using Maxwell-Wagner type polarization. In this mechanism, it is possible that the interface traps the injected charge, and then such a thin layer can modify the net effective polarization and/or relaxation behavior of the dielectric.[35]

Impedance spectroscopy of silicon nitride dielectrics was studied to gain insight into the electrical nature of the electrode-dielectric interface and/or dissimilar phases in the bulk of dielectrics. When the impedance spectrum of dielectrics is plotted as a function of the frequency, it is possible to monitor the electrical nature of dissimilar layers via their relaxation behavior (Cole-Cole). The electrical response can then be modeled in terms of an equivalent electrical circuit with different elements attributed to the various independent relaxation mechanisms. For example, Maxwell[35] proposed series layer models in which two phases were assumed to be stacked in layers parallel to the measurement electrodes (i.e., components in series). For this series arrangement, the impedance spectrum consists of two distinct semi-circles (or depressed semi-circles) with different relaxation times[37] (See Fig. 4.44). In the Maxwell-Wagner model, the effective real $\varepsilon'(\omega)$ and imaginary parts $\varepsilon''(\omega)$ of the complex permittivity are given by [36,37]

$$\varepsilon'(\omega) = \frac{1}{\boldsymbol{C}_0(\boldsymbol{R}_i + \boldsymbol{R}_b)} \frac{\tau_i + \tau_b - \tau + \omega^2 \tau_i \tau_b \tau}{1 + \omega^2 \tau^2}, \qquad (4.14)$$

$$\varepsilon''(\omega) = \frac{1}{\omega \boldsymbol{C}_0(\boldsymbol{R}_i + \boldsymbol{R}_b)} \frac{1 - \omega^2 \tau_i \tau_b - \tau + \omega^2 (\tau_i + \tau_b)\tau}{1 + \omega^2 \tau^2} \qquad (4.15)$$

$$\tau_i = \boldsymbol{C}_i \boldsymbol{R}_i, \quad \tau_b = \boldsymbol{C}_b \boldsymbol{R}_b, \quad \tau = \frac{\tau_i \boldsymbol{R}_b + \tau_b \boldsymbol{R}_i}{\boldsymbol{R}_i + \boldsymbol{R}_b}, \quad \boldsymbol{C}_0 = \varepsilon_0 \frac{\boldsymbol{A}}{\boldsymbol{t}}$$

where indices *"i" a*nd *"b"* describe the interfacial and bulk layers respectively. τ, τ_i, and τ_b are the effective relaxation times of the entire system, the interface, and the bulk respectively. R_i and R_b are the resistances of the bulk and interface respectively. One could imagine in the present studies such an interface at the electrode/sample.[36,37]

As shown in Figure 4.45 a), the Cole-Cole response of the F dielectric was measured at room temperature and on heating. The result doesn't satisfy the two layers in series model described by Maxwell at frequencies between 200 mHz and 100 kHz.

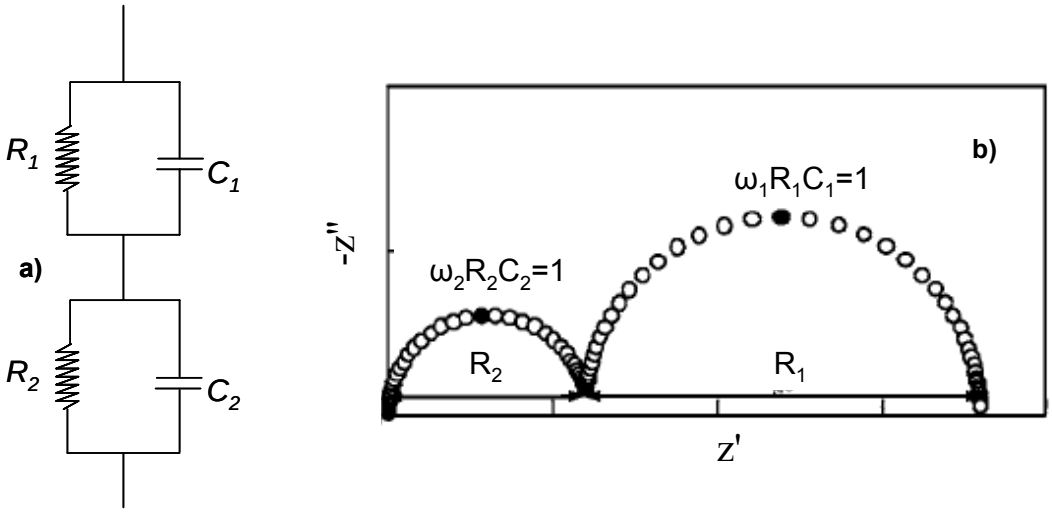

Figure 4.44 a) Two phase microstructural equivalent circuit **b)** Impedance spectrum of a two phase microstructure. R_1, R_2, C_1,and C_2 are the resistances and capacitances of the first and second phases, respectively. $\omega_1$and ω_2 are the angular frequencies of the first and second phases.[38]

Jonscher[4] reported the Cole-Cole response and the circuit model for a typical dielectric in which the real and imaginary components increase similarly without any loss peak towards low frequencies. Such behavior has been previously reported to occur if there is a distributed RC network. In such a case, the microstructure of this dielectric may be represented by the equivalent circuit shown in Figure 4.45 b). This would suggest that

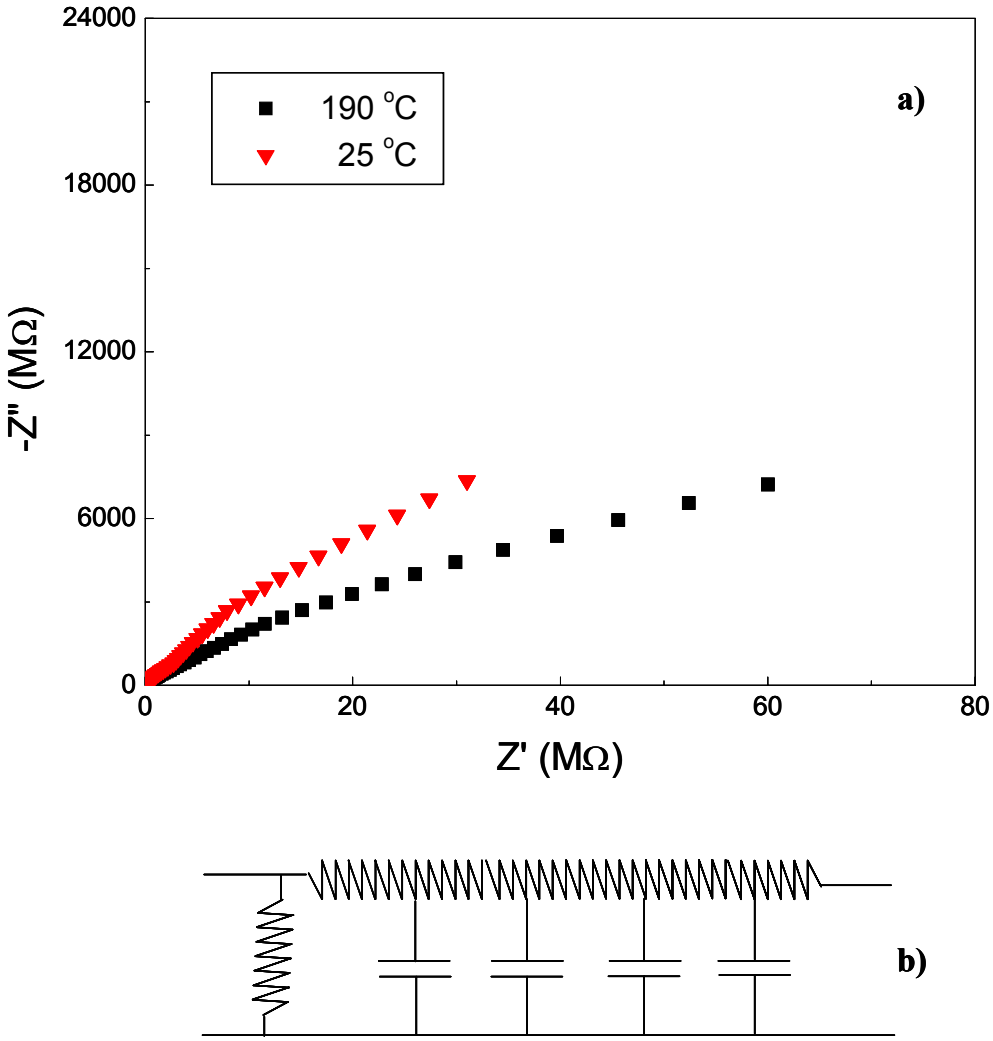

Figure 4.45 a) (Cole-Cole plot) Imaginary part of the impedance versus the real part in the F dielectric **b)** Distributed RC network circuit model.[4]

in F dielectrics not previously exposed to any high electric fields that there is no discrete surface layer.

Additionally, Figures 4.46 and 4.47 show the real and imaginary parts of the complex dielectric constant as a function of frequency in the standard and F dielectrics, respectively, measured using an ac signal of amplitude 1 volt. In order to understand the

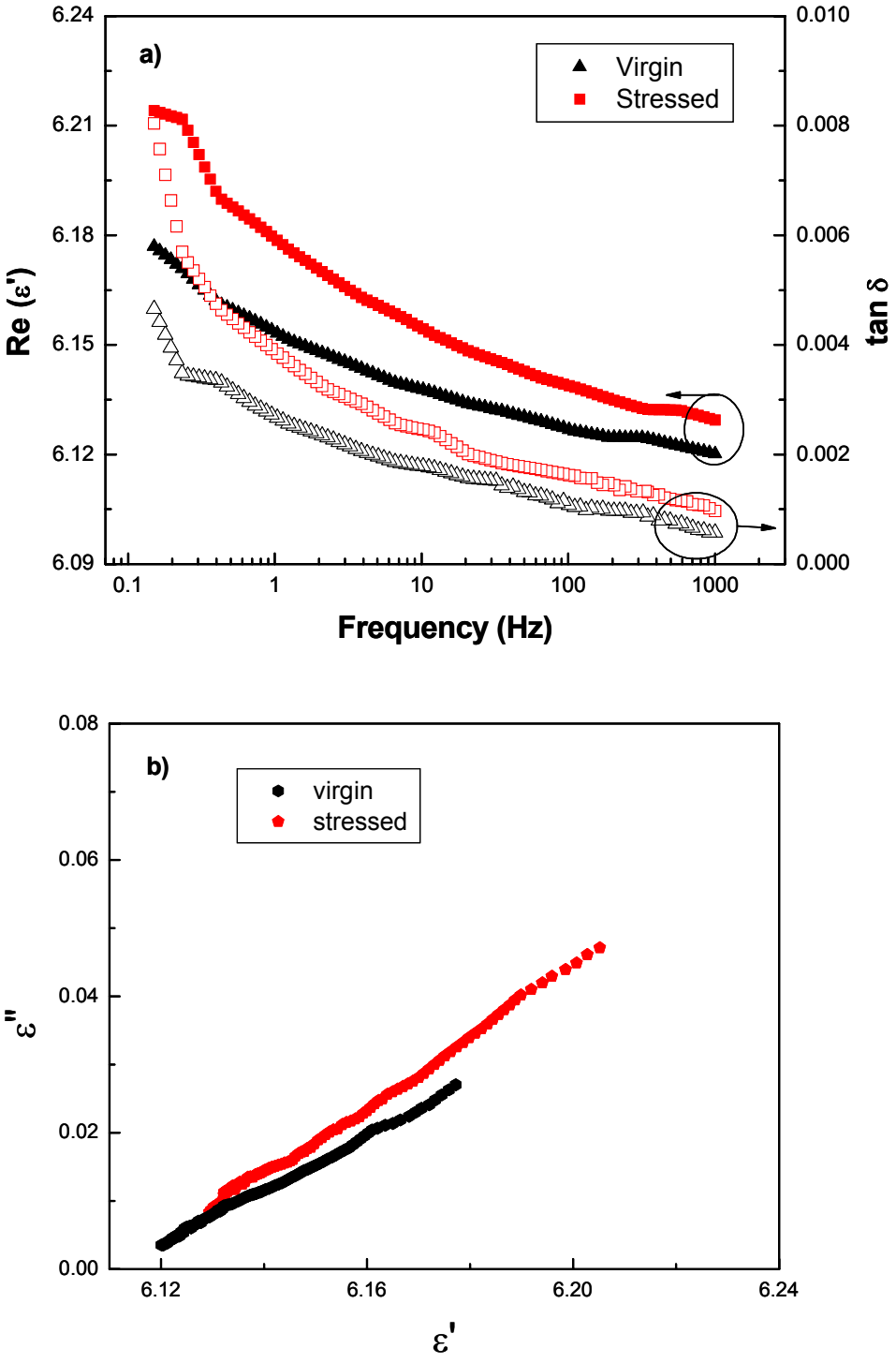

Figure 4.46 a) DC voltage-induced changes in the real part of the dielectric constant and loss in the standard dielectric as a function of the frequency **b)** Imaginary part of the dielectric constant versus the real part, measured in the standard dielectric before and after a DC field stressing (Cole-Cole).

effect of external DC stress on the charge trapping mechanism in the vicinity of the film-electrode interface, both types of films were stressed with a dc bias of 2000 kV/cm for 23 hours. The electric field was then removed for 1 day prior to measuring the dielectric dispersion. It can be seen from the figures that both the real and imaginary components of complex dielectric constant were increased after DC stress. These results clearly indicated that the DC stress modified the material; thereby the measured effective complex dielectric properties were changed. As depicted in Figures 4.46 b) and 4.47 b), the Cole-Cole response of dielectrics showed that there was no discrete surface layer formation after exposing films to a high electric field. However, the Cole-Cole response of the F dielectric changed form after application of a DC stress (see Fig. 4.47-b). The real nature of this behavior was described in the following paragraphs with additional experimental data.

Furthermore, the trapped charge density (Δn) of the dielectrics can be found by [39]

$$\Delta n = \frac{|C_{stressed} - C_{virgin}|V}{e \times A} \qquad (4.16)$$

where *e*, A, C, and V are the electronic charge, electrode area, capacitance, and ac bias, respectively. Figures 4.48 and 4.49 show the equivalent electronic trapped charge density for the standard dielectric and the F dielectric respectively. It can be seen clearly that the trapped charge density was increased in both dielectrics; however in the F dielectric the equivalent trapped electron charge density was higher after DC stress compared to the standard dielectric.

In order to understand the effect of DC stress on the long term degradation of dielectrics, both types of films were stressed with a dc bias of 3750 kV/cm for 5 hours to 22 hours prior to measuring the dielectric dispersion. As shown in Figure 4.50, plots of ε"

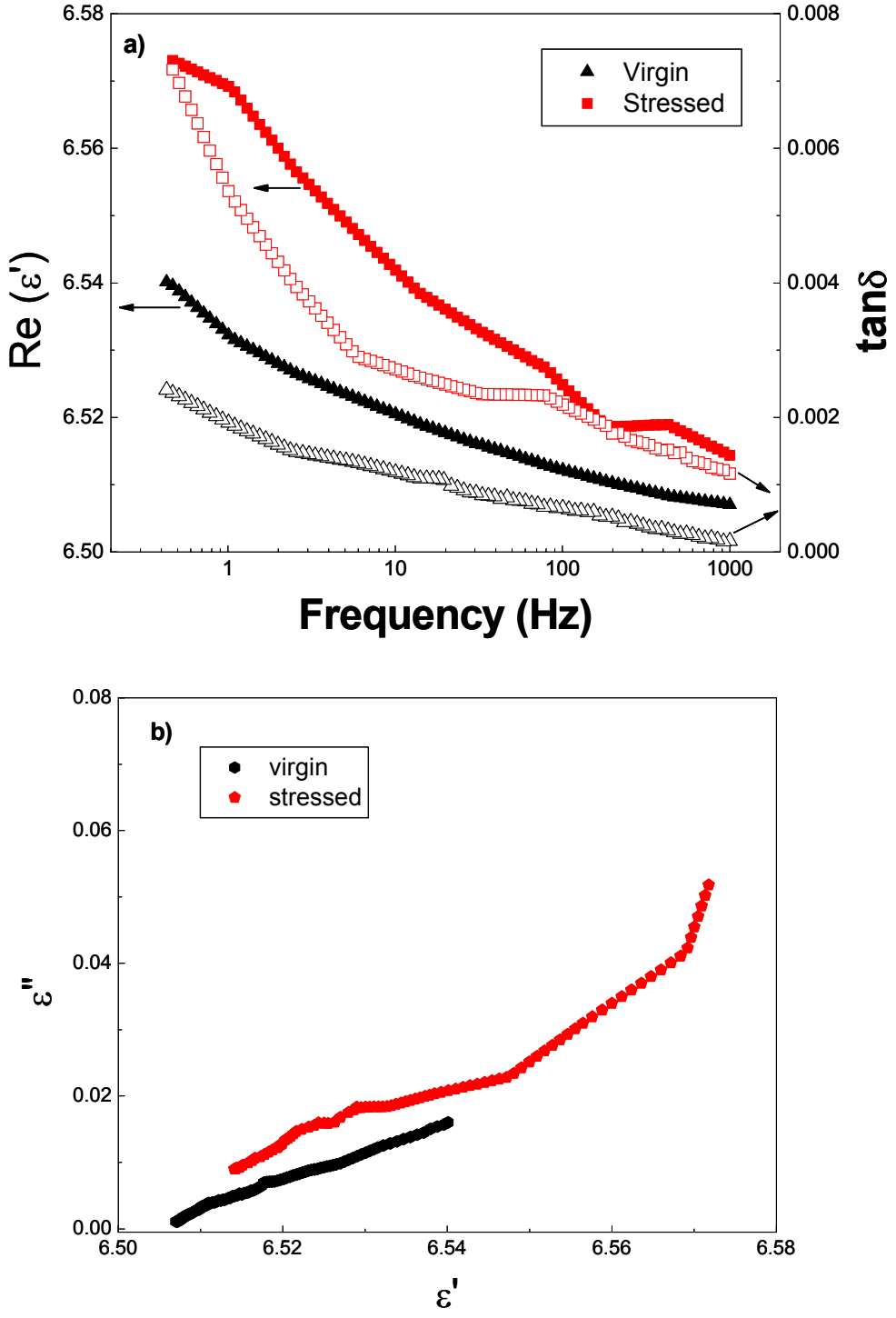

Figure 4.47 a) DC voltage-induced changes in the real part of the dielectric constant and loss in the F dielectric as a function of the frequency **b)** Imaginary part of the dielectric constant versus the real part, measured in the F dielectric before and after a DC field stressing (Cole-Cole).

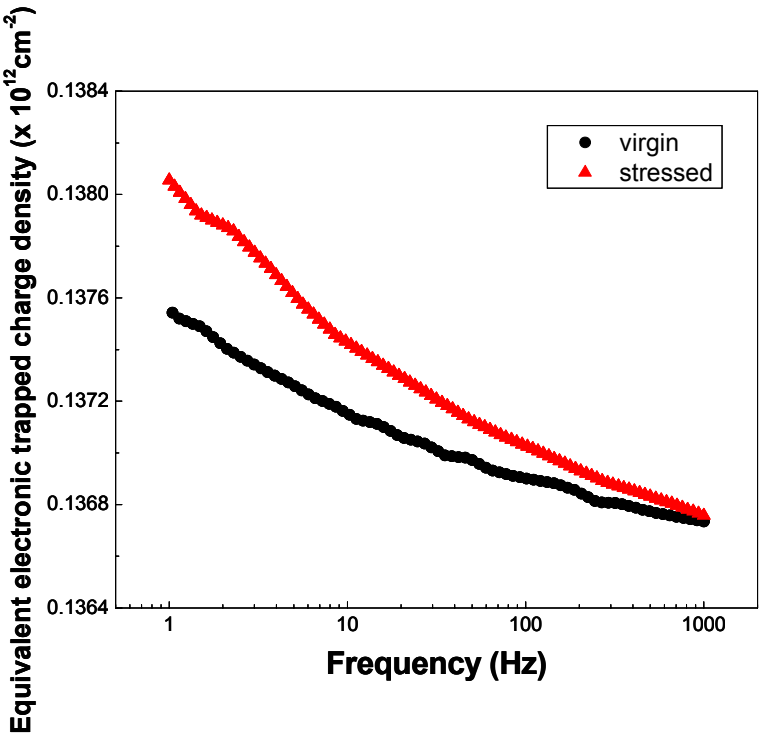

Figure 4.48 Equivalent electronic trapped charge density in the standard dielectric.

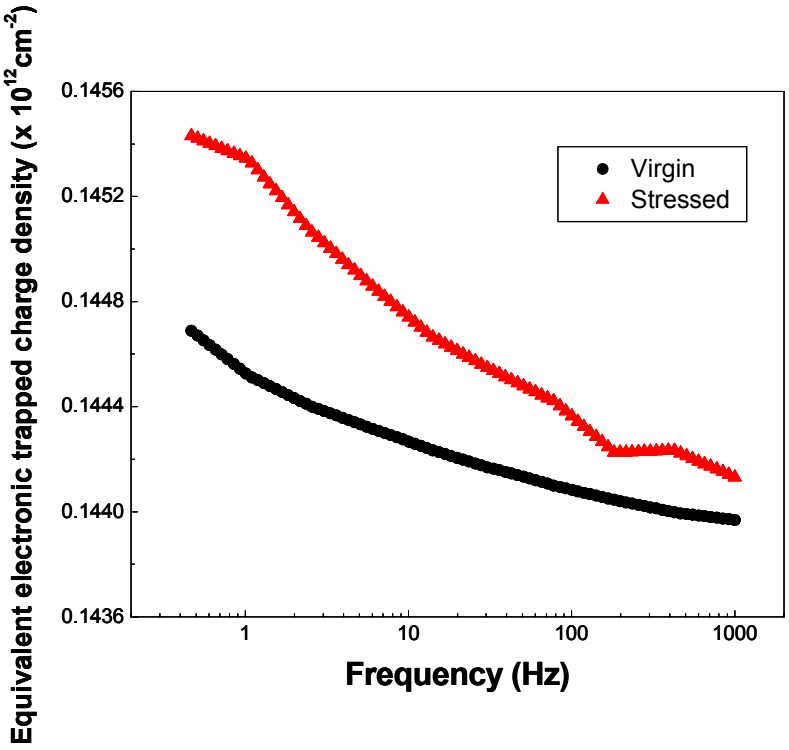

Figure 4.49 Equivalent electronic trapped charge density in the F dielectric.

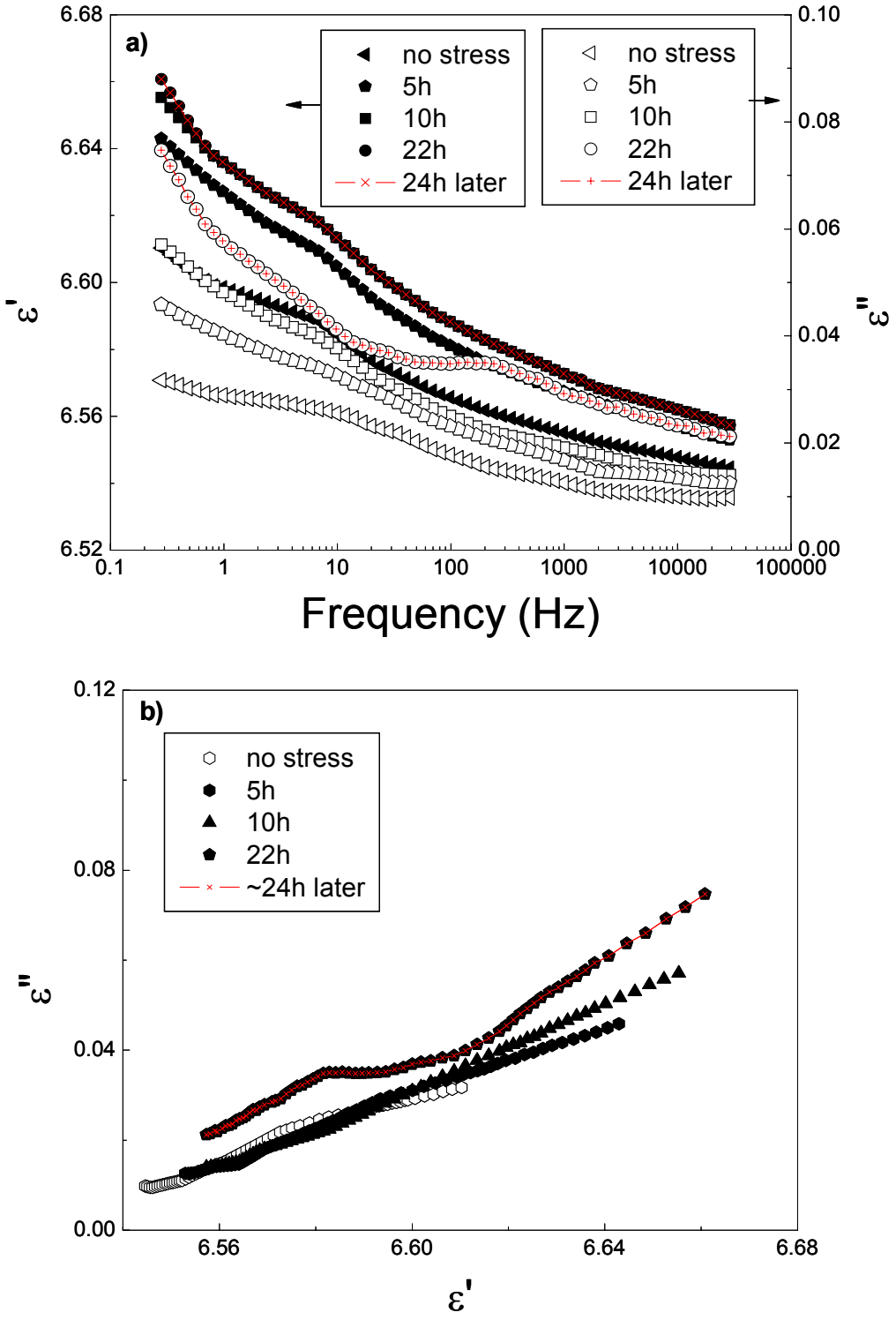

Figure 4. 50 a) Real and imaginary part of the dielectric constant were measured as a function of frequency for different stressing times in the F dielectric **b)** Imaginary part of the dielectric constant, ε", versus the real part, ε', measured in the F dielectric after a DC field stressing.

versus ε' shift up and to the right after application of an external DC bias stress for both dielectrics. In particular, the Cole-Cole response of the F dielectric was degraded after long stressing times (e.g., 22 hr) and showed a permanent change with no recovery. Thus, the data taken 24 hours after the bias was removed was superimposed on the 22 hours stressing data. However, as shown in Figure 4.51, the ε' and ε" of the standard dielectric partially relaxed after ~24 hours with no field applied. These changes in the dielectric are likely to be correlated with the ultimate switch lifetime.

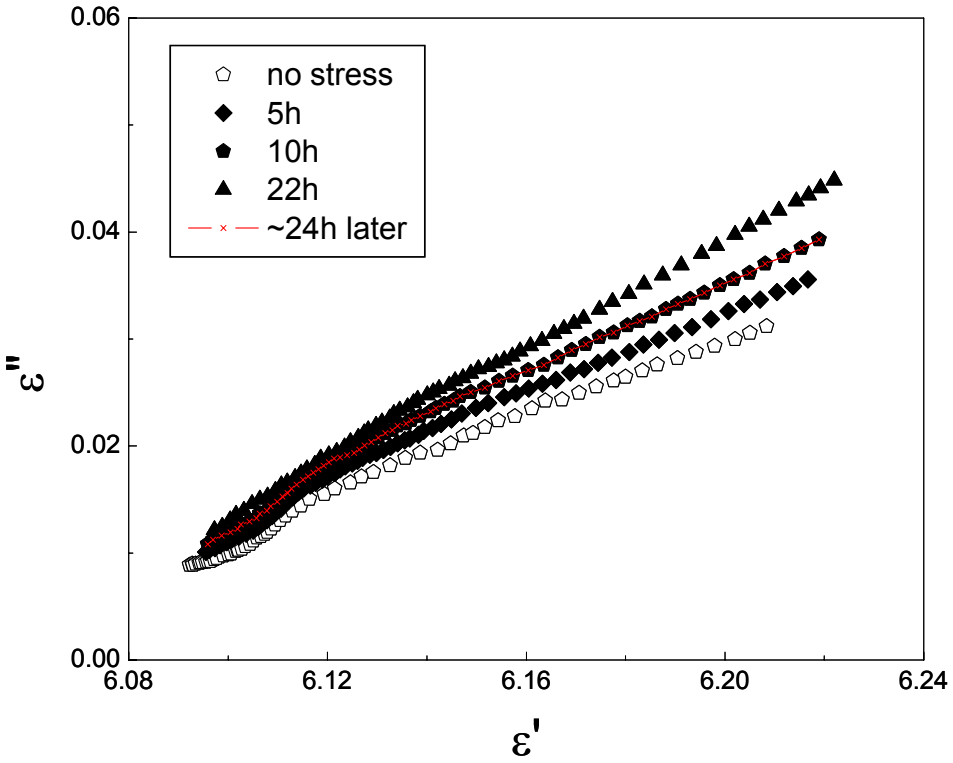

Figure 4. 51 Imaginary part of the dielectric constant, ε", versus the real part, ε', measured in the standard dielectric after a DC field stressing. The 24 hours later data refer to a measurement made 24 hours after the 22 hours voltage stress.

In addition, the Cole-Cole response of the F dielectric was studied after removal of the

DC field in order to monitor the recovery of the dielectric dispersion. For that reason, the imaginary and real part of dielectric constant was measured as a function of the frequency (200 mHz-100 kHz) before and immediately after a DC electric field stress of 3750 kV/cm for different stressing times (5 - 20 hours). As depicted in Figure 4.52 d), the Cole-Cole response in the F dielectric shifted to the right and up after 20 hours of electric field stress with no recovery. As field stressing time decreased, the time required for recovery decreased rapidly, so that recovery was essentially complete within a few minutes after 5-10 hours of stressing (Fig. 4. 52 a-b). The time required for recovery will have a strong impact on the failure of capacitive devices.

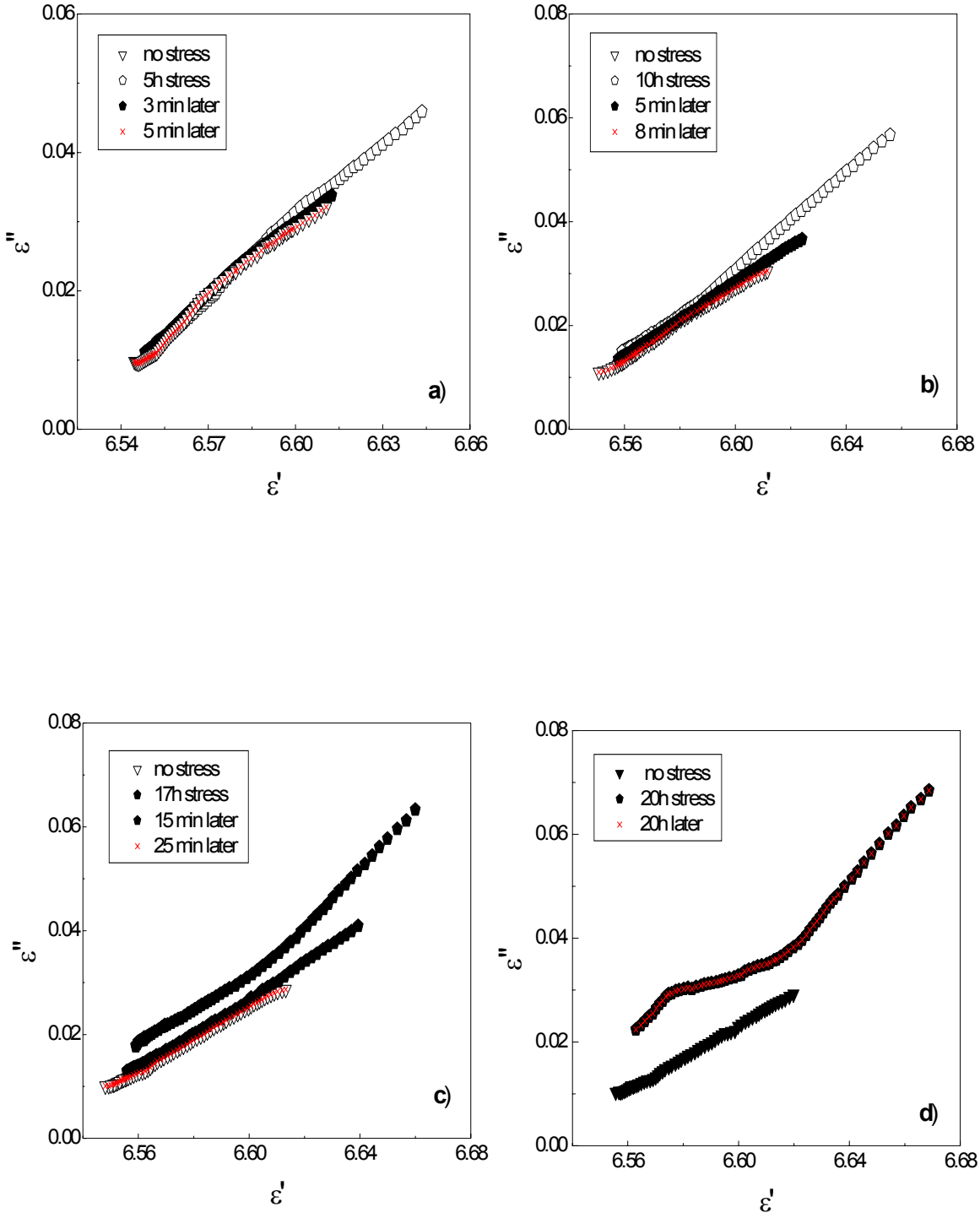

Figure 4.52 (a-d) Imaginary part of the dielectric constant, ε'', versus the real part, ε', measured in the F dielectrics after a DC field removal for different stressing times. The original field stress was 3750 kV/cm for different stressing times. The data are compared with results from an unstressed film.

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Chapter 5

Conclusions and Future Work

5.1 Conclusions

5.1.1 Standard Dielectric

The current-voltage response of the standard dielectric as a function of time provided only information on transient currents. Therefore, the steady-state currents couldn't be achieved for further study of conduction mechanisms. These currents showed electrode dependence for both polarities and up to the highest electric field of 4 $MV.cm^{-1}$. The magnitude of these current was the largest for the Pt, the smallest for the Al, and intermediate for Ti-Au top electrodes. In addition, the current density increased after a long term stress (23 hours) at electric field of $4MV.cm^{-1}$.

5.1.2 F Dielectric

The current density of this dielectric was found to be higher than that of the standard dielectric at all studied electric fields (0-2560kV/cm). Different top electrodes with different work functions were also studied to understand the electrode effect on leakage current response. However, the observed currents were similar for all electrodes at both polarities. In addition, silicon nitride films for different thicknesses (0.16μm, 0.25μm, and 0.4μm) were studied at electric field ranges between 0kV/cm and 2560 kV/cm. For this study, it was found that the current density was thickness independent.

Charging currents of the F dielectric as a function of the time were studied to define leakage current regimes at constant electric fields. These currents were in the

steady-state currents regions at electric fields up to 1MV/cm and enabled the study of conduction mechanisms. In these field regions, the dynamic dielectric constant of the F dielectric was obtained by fitting data to the Poole-Frenkel equation. These values were estimated to be 3.67±0.04, 3.28±0.06, and 3.4±0.03 for the Ti-Au, Pt, and Al top electrodes, respectively. The optical dielectric constant for the F dielectric was separately measured to be 4.4 at 630nm using ellipsometry. The calculated dynamic dielectric constant was close to its optical values, which confirmed Poole-Frenkel conduction at field levels above 1MV/cm. In addition, the I-V characteristic of capacitive switch with the F dielectric demonstrated results similar to those on MIM capacitors. The dielectric constant was found to be 2.84±0.065 from the capacitive switch data using a Ti-Au bridge.

From the studied temperatures (298- 423K) at electric field of 2.32MV/cm, the Poole-Frenkel barrier heights were 0.84±0.015eV, 0.86±0.023eV, and 0.83±0.014eV for Al, Pt, and Ti-Au electrodes, respectively. Furthermore, the pre-exponential factors (C) were calculated to be $2.52(\pm0.154)\text{x}10^{-4}$ $AV^{-1}m^{-1}$ for Ti-Au, $2.71(\pm0.16)\text{x}10^{-4}$ $AV^{-1}m^{-1}$ for Al, and $2.85(\pm0.25)\text{x}10^{-4}$ $AV^{-1}m^{-1}$ for the Pt top electrode. These are consistent with a N/Si ratio between 1.1 and 1.2.[3] The current density of the F dielectric demonstrated no change after 24 hours at an electric field of 2.6 $MV.cm^{-1}$. In contrast, the real part of the dielectric constant and dielectric loss increased when it was measured using AC signals at frequencies ranges between 150 mHz and 1 kHz after DC field stress of 2 $MV.cm^{-1}$ for 18 hours. This suggests that the AC measurements may be a superior means of quantifying changes in the dielectric characteristic of charge trapping. Additional work should be done to confirm this.

5.2 Recommendations for Future Work

5.2.1 Transient Current Study of Dielectrics

Steady-state currents couldn't be achieved for a 0.25μm thick standard dielectric at electric fields <4MV/cm. Hence, the observed currents are polarization currents. In order to reach steady-state regions for this dielectric, either thinner films (<0.25 μm) or higher electric fields (>4MV/cm) are required. It would be useful to find out why the polarization currents are electrode dependent for both standard (<4MV.cm^{-1}) and F dielectrics (slightly, at low fields). Engineering of the electrode barrier heights may become progressively more important in controlling charge injection as the operating voltages of switches are brought to lower levels, so that the field level in the dielectric drops to levels below that characteristic of Poole-Frenkel conduction in Si-rich silicon nitrides. Unfortunately, though, it is not clear that this will change the barriers associated with detrapping of injected charges, so there may be no long-term reliability improvement to be achieved by operating in the polarization current regime.

5.2.2 Alternative Candidate Materials for Improving Capacitive MEMS Switches

The existing theories propose that dangling bonds form states in the band gap and cause charge trapping to occur in silicon nitride.[4] It has also been proposed that the Poole-Frenkel potential barrier height is decreased by introducing more silicon into the silicon nitride.[3] As shown in Figure 5.1, the Si-rich composition has a smaller band gap than the N-rich composition.[5] In addition, the Poole-Frenkel barrier heights of Si-rich compositions are smaller than those of N-rich compositions. Lower barrier heights increase the rate of emission of trapped charges into the conduction band of insulator due

to the lower activation energy.

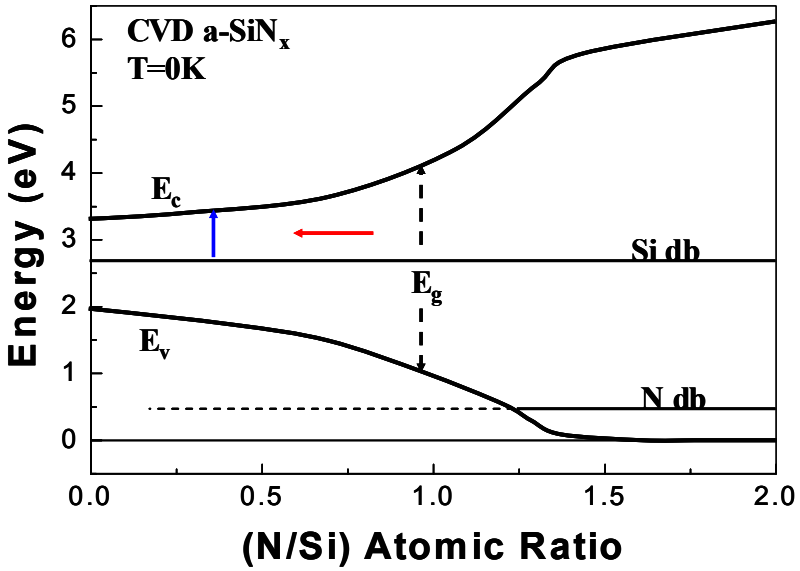

Figure 5.1 Energy band gap diagram of silicon nitride as a function of N/Si ratio proposed by Warren *et al.* E_c, E_v , Si db, and N db are conduction band energy , valance band energy, Si dangling bond energy, and nitrogen dangling bond energy.[5]

Alternative materials with smaller band gaps and smaller trap depth will be attractive to study in order to reduce stiction in capacitive MEMS switches. As seen in Figure 5.1, the band gap of stoichiometric silicon nitride is about 5.1±0.2eV. Table 5.1 shows a list of materials with their band gap values.[6] As depicted in Table, $SrTiO_3$, $PbTiO_3$, $PbZrO_3$, Ta_2O_5, $SrBi_2Ta_2O_9$, and TiO_2 offer smaller band gap than that of Si_3N_4. Among these materials, $SrTiO_3$ has been investigated for capacitive switch applications by another institute.[7] An on-off capacitance ratio of > 600 has been demonstrated using capacitive switches with a 190nm thick $SrTiO_3$ as an isolation layer. The overall actuation voltages were extremely low, between 8 and 15 volts, which yielded better

lifetime (no information was given on the maximum number of operation cycles) due to in the reduction of the electric field across an insulator layer.

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Table 5.1 Band gaps, charge neutrality levels above the valence band (CNL), dielectric constant (ε_∞), pinning parameter (S), electron affinity (EA), and conduction band offset (CB) on Si for each oxide* were experimentally estimated, or calculated for different materials.[6]

	Gap (eV)	CNL (eV)	ϵ_∞	S calculated	EA (eV)	Calculated CB offset (eV)
Si	1.1	0.2	12		4.0	
SiO_2	9		2.25	0.86	0.9	3.5 (exp)
Si_3N_4	5.3		3.8	0.51	2.1	2.4 (exp)
$SrTiO_3$	3.3	2.60	6.1	0.28	3.9	−0.1
$PbTiO_3$	3.4	1.90	6.25	0.31	3.5	0.6
$BaZrO_3$	5.3	3.7	4	0.53	2.5	0.8
$PbZrO_3$	3.7	2.6	4.8	0.4	3.2	0.2
Ta_2O_5	4.4	3.3	4.84	0.40	3.2	0.36
$SrBi_2Ta_2O_9$	4.1	3.3	5.3	0.35	3.3	0.15
TiO_2	3.05	2.2	7.8	0.18	3.9*	0
ZrO_2	5.8	3.6	4.8	0.41	2.5*	1.4
HfO_2	6	3.7	4	0.53	2.5*	1.5
Al_2O_3	8.8	5.5	3.4	0.63	1*	2.8
Y_2O_3	6	2.4	4.4	0.46	2*	2.3
La_2O_3	6*	2.4	4	0.53	2*	2.3
$ZrSiO_4$	6*	3.6	3.8	0.56	2.5*	1.5
$HfSiO_4$	6*	3.6	3.8	0.56	2.5*	1.5

5.2.3 Technique to Characterize Charge Trapping in Silicon Nitride

As an additional electrical characterization technique, deep-level transient spectroscopy (DLTS) can be studied to better characterize charge trapping in the silicon nitride. DLTS was introduced by Lang [8] as a powerful tool for characterizing the charge trapping in GaAs. This technique provides information about the majority and minority carrier trap concentrations, energy levels, and capture rates.[8] It has advantages over the

thermally simulated currents technique (TSC) such as its ability to distinguish between majority and minority carrier traps (holes and electrons). As shown Figure 5.2, the activation energy (0.44 eV and 0.76 eV) of hole traps were measured in GaAs for two different samples (A and B) using DLTS spectra. The hole trap concentration was calculated to be $14x10^{-4}$ cm^{-3} for both samples. In addition, Figure 5.2 shows DLTS spectra for hole and electron traps for different injection times in n-GaAs.

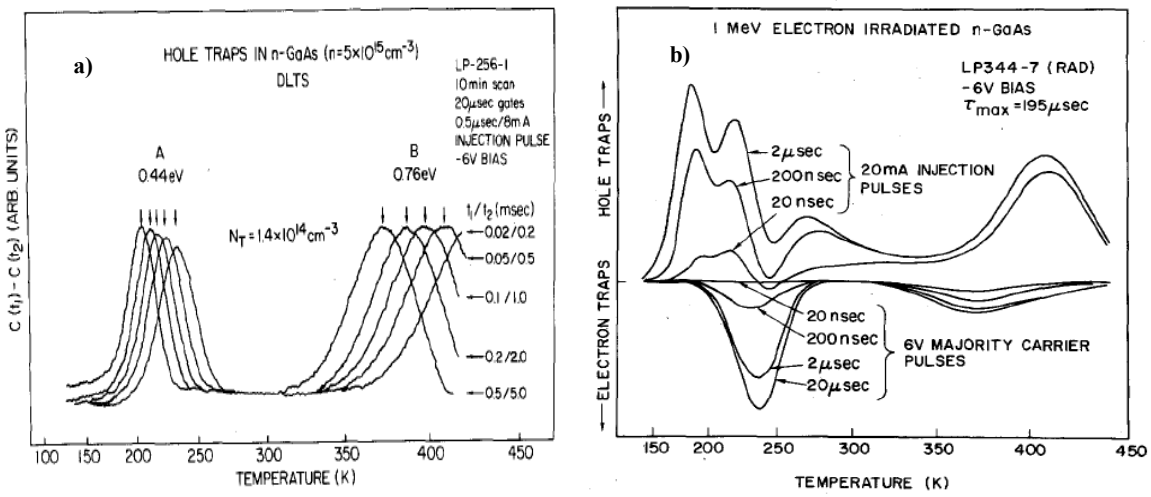

Figure 5.2 a) DLTS spectra for hole traps in n-GaAs **b)** DLTS spectra for hole and electron traps in n-GaAs. $C(t_1)$ is the capacitance at t_1-time and $C(t_2)$ is the capacitance at t_2-time.[8]

Application of this tool to silicon nitride films for capacitive switches would enable the trap concentration and energy distribution to be determined. It would be particularly interesting to measure films before and after high field stressing. This might enable those traps, which are lifetime limiters in switches to be identified. This, in turn, might enable better deposition conditions for the dielectric to be developed without requiring a full switch fabrication run.

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