

Realizing Linear Synaptic Plasticity in Ion-Gated MoS₂ Transistors for Enhanced Neuromorphic Computing Performance

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To overcome the von Neumann bottleneck and increase power efficiency in computation, neuromorphic computing has been considered, which has the capability for parallel computing, long-term potentiation, and adaptive learning for developing energy efficient neural networks.¹ Electric double layer (EDL) gated transistor uses ions within an electrolyte to induce high carrier density (10^{14} cm^{-2}) in the channel, and its short term and long term ionic responses resemble a biological synapse, making it a promising platform for synaptic applications such as artificial synapses and neurons.² The accuracy, computational demands, and simplicity of training neural networks depend significantly on a linear synaptic weight response (or plasticity), i.e. a proportionate conductance update in response to input signals.^{3,4} However, achieving such linearity in EDLTs with fixed-magnitude input pulses remains a significant challenge.^{5,6} In this work, we identify the root cause of nonlinearity through finite-element modeling based on modified Nernst–Poisson–Planck equations,⁷ revealing that the competition between EDL formation and dissipation rates depends on the local ionic concentration. We experimentally applied ten-pulse trains (2–10 Hz) to MoS₂-based EDLTs gated with PEO:LiClO₄ and observed nonlinear conductance updates. To address this, we developed the Linear Ionic Weight Update Solver (LIWUS), a Python-based predictive model trained on measured voltage- and current-dependent rates, to generate optimized incremental pulses that achieved linear weight modulation. Integration of this model into a three-layer artificial neural network trained on the MNIST dataset resulted in higher classification accuracy and lower error rates compared to networks trained using nonlinear updates. These findings highlight the critical importance of linear and symmetric weight modulation in neuromorphic systems and demonstrate a viable pathway to improve learning performance in spiking neural networks through tailored STDP-compatible pulse schemes.

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