Reducing Variation of Graphene FETs via Recessed-Gate and hBN Integration

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Abstract: The International Roadmap for Devices and Systems (IRDS) 2023 identifies two-dimensional (2D) materials as critical channel candidates for CMOS extension by 2028 and highlights 2D devices for beyond-CMOS applications [1]. Achieving these goals requires concerted efforts at the research, development, and manufacturing levels. Leading semiconductor companies, including TSMC and IMEC, have demonstrated fabricated devices based on 2D materials, signaling a shift toward high-volume manufacturable 2D technologies.

Silicon CMOS technologies are approaching physical and performance scaling limits, prompting the investigation of novel materials such as graphene. Graphene, with its exceptional carrier mobility (~250,000 $cm^2V^{-1}s^{-1}$) and atomically thin structure [2], offers a pathway to enhanced electrostatic control and high-frequency device performance. Although graphene field-effect transistors (GFETs) have demonstrated superior performance compared to silicon transistors at equivalent technology nodes, their widespread adoption has been hindered by significant device-to-device variability. Key sources of variability include contact resistance, dielectric/graphene interface quality, and graphene uniformity.

This work addresses these critical issues by systematically integrating a monolayer hexagonal boron nitride (hBN) (~0.45 nm) as the gate dielectric, replacing the conventional 15-nm Al_2O_3 layer, and by planarizing the aluminum gate using chemical mechanical planarization (CMP). Process cross-sections of these fabrication improvements are presented to highlight the structural evolution toward more uniform devices.

Experimental results demonstrate a substantial reduction in device variability: the standard deviation of extracted hole mobility decreased from 75% to 18%, while device yield improved significantly from 14.8% to 65.1%. The Dirac point shifted closer to zero volts (from ~8 V to 0.7 V), and the contact resistance was reduced from 2.9 kΩ·μm to 0.6 kΩ·μm. The improvements in the gate/dielectric and dielectric/channel interfaces, attributed to hBN integration and gate planarization, reduced interface trap density and enabled more consistent device characteristics. Consequently, the cutoff frequency (f_t) improved from 0.3 GHz to 0.9 GHz, highlighting the potential for high-frequency applications.

Although the performance of "hero" devices—those with peak metrics—was similar across different device structures (Al_2O_3 on raised gate, hBN on raised gate, hBN on recessed gate), overall device uniformity and reproducibility were significantly improved with the hBN-on-recessed-Al approach. These improvements are critical to enabling future scalable, reliable

graphene-based device technologies for applications in RF electronics, neuromorphic computing, photonic integrated circuits, and quantum technologies.

Nevertheless, challenges remain. Further efforts are required to improve intrinsic graphene mobility and to continue lowering the variability of contact resistance. Future directions include employing advanced encapsulation techniques and refined fabrication processes to further enhance device performance and manufacturability at the wafer scale.

[1] M. C. Lemme, D. Akinwande, C. Huyghebaert, and C. Stampfer, "2D materials for future heterogeneous electronics," *Nat Commun*, vol. 13, no. 1, p. 1392, Mar. 2022, doi: 10.1038/s41467-022-29001-4.

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